Title

Multi-Valued Majority Logic Circuits Using Spin Waves

Authors

Sankara Narayanan Rajapandian, *University of Massachusetts Amherst* Follow

Document Type

Open Access

Degree Program

Electrical & Computer Engineering

Degree Type

Master of Science in Electrical and Computer Engineering (M.S.E.C.E.)

Year Degree Awarded

2013

Month Degree Awarded

September

Keywords

Spin Wave, Multi-valued logic, Majority logic

Abstract

With increasing data sets for processing, there is a requirement to build faster and smaller arithmetic circuits. One of the ways to improve the performance of higher order arithmetic units is to reduce the carry propagation levels. Multi-valued logic enables this by reducing the number of digits required to represent a range of numbers. Area reduction is also obtained through fewer operations and signals required to realise a function.

Though theoretically multi-valued logic has these advantages, implementation of the multi-valued logic using CMOS has not been efficient. The main reason is because multi-valued logic is emulated in CMOS using binary switches. Two main approaches are followed in CMOS in implementing multi-valued logic using CMOS. Voltage mode logic, where the logic states are encoded using the node voltages suffer from low noise margins and limitation of radix due to the power supply. Current mode logic, where the branch currents are used to represent the logic levels suffer from high power consumption due to static current flow and requirement of restoration devices. The mindset of the post-CMOS approaches explored so far for multi-valued logic circuit design has been to replace the CMOS switches with their novel nano switches. Hence they too suffer from the same issues as CMOS implementation.

Our value proposition is through the use of a truly multi-state device based on electron spin. Spin waves, which are a collection of electron spins of an atom enables multi-valued logic by allowing encoding information in the amplitude and phase of the wave.Another advantage of the spin wave fabric is that the computation is through wave propagation and interference which does not involve any movement of charge. This enables building low energy,smaller and faster multi-valued circuits. In this thesis, implementation of the basic building blocks of multi-valued logic using these novel spin wave based devices is shown. Building of arithmetic circuits like adders using these building blocks have also been demonstrated. To quantify the benefits of spin wave based multi-valued circuits, they are benchmarked with CMOS. For 32-bits, our projected comparisons show a 5X increased performance, 125X area improvement and 1717X power reduction for hexa-decimal spin wave based adders compared to binary CMOS. Similarly there is a 4X increase in performance of hexa-decimal SPWF multiplier compared to CMOS for 16 bits. Finally, we have implemented the I/O circuits for smooth interface between binary CMOS and multi-valued SPWF logic.

First Advisor

Csaba Andras Moritz