



## Masters Theses 1896 - February 2014

Off-campus UMass Amherst users: To download campus access theses, please use the following link to log into our proxy server with your UMass Amherst user name and password.

Non-UMass Amherst users: Please talk to your librarian about requesting this thesis through interlibrary loan.

Theses that have an embargo placed on them will not be available to anyone until the embargo expires.

# Functional Verification of Arithmetic Circuits using Linear Algebra Methods



Mohamed Abdul Basith Ameer Abdul Kader, *University of Massachusetts - Amherst*



Document Type
Open Access

Degree Program
Electrical & Computer Engineering

Degree Type
Master of Science in Electrical and Computer Engineering (M.S.E.C.E.)

Year Degree Awarded
2011

Month Degree Awarded
September

Keywords
Functional Verification, Arithmetic Circuits, Linear Algebra, SMT, Arithmetic bit-level, Equivalence checking

Abstract
This thesis describes an efficient method for speeding up functional verification of arithmetic circuits namely linear network such as wallace trees, counters using linear algebra techniques. The circuit is represented as a network of half adders, full adders and inverters, and modeled as a system of linear equations. The proof of functional correctness of the design is obtained by computing its algebraic signature using standard linear programming (LP) solver and comparing it with the reference signature provided by the designer. Initial experimental results and comparison with Satisfiability Modulo Theorem (SMT) solvers show that the method is efficient, scalable and applicable to complex arithmetic designs, including large multipliers. It is intended to provide a new front end theory/engine to enhance SMT solvers.

Advisor(s) or Committee Chair
Ciesielski, Maciej