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An Electronically Reconfigurable Three Band Low-Noise Amplifier in 0.5 µm GaAs pHEMT Technology

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Document Type
Open Access

Degree Program
Electrical & Computer Engineering

Degree Type
Master of Science in Electrical and Computer Engineering (M.S.E.C.E.)

Year Degree Awarded
2011

Month Degree Awarded
May

Keywords
RFIC, MMIC, LNA, Reconfigurable, IC

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Abstract
State-of-the-art RF front-end circuits are typically designed to operate at a single frequency. With an increasing number of available wireless standards, personal mobile communication devices require an increasing number of individually designed RF circuits. To save space and cost, one alternative possibility is to reuse much of the circuitry by utilizing electronically reconfigurable topologies. The ubiquitous low-noise amplifier

is one of the many circuits that can be redesigned with the reconfigurable aspect in mind. In this thesis, previous work in reconfigurable LNAs is reviewed as well as a brief comparison of CMOS and GaAs processes used for RF amplifiers. Three new reconfigurable LNA topologies are also presented. The first two topologies, based on the common-gate stage and synchronous filters, are investigated but not manufactured. The third design, based on the cascode topology, was manufactured in a 0.5 µm GaAs process with enhancement-mode and depletion-mode pHEMTs. The LNA features 12.7 dB, 13.6 dB, and 13.9 dB of gain and noise figures of 2.7 dB, 3.5 dB, and 4.2 dB at 2.5, 3.6 and 5.8 GHz, respectively. The LNA draws 41 mA from a 3.3 V supply.

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