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深亚微米电路NMOS器件HCI退化建模与仿真

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摘要　提出一种深亚微米NMOSFET的热载流子注入下漏电流退化模型及其电路退化仿真方法．该模型将亚阈区、线性区和饱和区的漏电流退化行为统一到一个连续表达式中，避免了分别描述时由于模型不连续而导致的仿真不收敛问题．并且在模型中对亚阈区的栅偏依赖现象进行建模，提高了模型描述器件退化的准确度．用基于0.25μm工艺的NMOS器件对模型进行了验证，测试数据与仿真结果吻合得很好．

关键词　深亚微米NMOSFET　热载流子注入退化　ΔI_d模型　电路可靠性

分类号 TN386.6

Modeling and simulation of the HCI degradation model for the NMOSFET in deep submicron circuits

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Abstract

A model of drain current degradation of DSM NMOSFET devices induced by HCI and implementation in circuit reliability simulation is proposed. The model unifies the subthreshold, linear and saturation regions into a continuous equation, which a voids the simulation convergence problem due to the discontinuous model. And the gate bias dependency in the subthreshold region is also modeled for improved accuracy. The model has a high accuracy for SMIC on their 0.25μm technologies. The simulation method in this paper has been applied to the XDRT circuit reliability simulator.

Key words　deep submicron NMOSFET　HCI degradation　ΔI_d model　HCI circuit reliability simulation

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