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论文

面向测试的SOC核间互连网络约简算法

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摘要：

随着集成电路的制造工艺和工作频率已经进入了深亚微米和吉赫兹时代，片上系统核间互连总线的串扰测试已经成为不容忽视的问题．通过对片上系统核间互连总线特征的研究，提出了一种面向测试的片上系统核间互连总线的约简算法．该算法首先对核间互连的拓扑结构进行描述，建立互连关系矩阵，并以受害线为根结点构建互连关系分级树，根据测试精度去掉多余的攻击线．其次，根据互斥算法对包含三态双向驱动源的互连线进行筛选，确定施加激励的互连线．经过约简后的互连网络可根据测试矢量生成算法生成测试矢量集．该算法使生成的测试矢量集大大缩小，并提高了测试效率．

关键词： 片上系统 核间互连 三态双向网络

Study of the reduction algorithm of SOC inter-core interconnects for testing

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Abstract:

With the manufacturing technology and operation frequency of VLSI entering the era of DSM and GHz, the crosstalk of SOC inter-core interconnects can not be ignored anymore. A reduction algorithm for core-external interconnect is presented based on characteristics of the interconnect bus of SOC. Any topology of inter-core interconnects is described first and an interconnect relationship tree is built. Unwanted aggressive interconnects could be cut off according to the accuracy of test. Interconnects with the tri-state and bi-direction driving source are sifted according to the mutex algorithm. Test patterns are generated for these interconnects after sifting according to the TPG algorithm. The test set is decreased and test efficiency is improved.

Keywords: system on chip inter-core interconnects tri-state bi-directed nets

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