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网络、通信与安全

片上通信结构——共享总线和NoC的分析与比较

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摘要 采用模块化方法对集中式仲裁共享总线和二维网格片上网络（Network on Chip，NoC）的硬件开销和延迟进行了数学上的分析。在此基础上，通过可综合Verilog代码对这两种片上通信结构在RTL级进行描述，并建立了这两种通信方式的周期准确级的功能验证和性能分析环境。结果表明，在同样工艺条件下，共享总线的面积与NoC相比相当小；但对于大规模片上系统通信，NoC的吞吐效率及带宽明显优于共享总线。

关键词 共享总线 NoC 路由 片上通信
分类号

Performance analysis and comparison of **s**hared **b**us and NoC on **c**hip **c**ommunication **a**rchitecture

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Abstract
The paper analyzes some common features of the shared bus with centralized arbitration and two dimensional NoC through a modular method.First the two communication architectures are described with the synthesized Verilog language，and two function verification and cycle accurate performance analysis environments are also implemented to evaluate their performance.The experiment result shows the shared bus is considerably smaller in area than NoC for the same technology，but the throughput efficiency and bandwidth of NoC obviously outperforms the shared bus for large-scale on-chip communication.

Key words shared bus Network on Chip（NoC） router on-chip communication

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