研究论文

针对定点小数乘法器位宽的优化算法

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摘要：

提出了一种针对定点小数乘法器位宽的低功耗优化算法，阐述了其基本原理及实现方案，并通过现场可编程门阵列(FPGA)测试，验证了该算法的低功耗优化效果．在算法上，其优化指标为小数乘法器内部寄存中间运算结果的寄存器位宽；而在实现技术上，解决了目前低功耗设计中算法自身逻辑单元引入被优化系统，从而降低了系统优化效果的问题．该算法适用于对含有大量小数乘法运算的系统进行低功耗优化，例如数字信号处理、数字滤波器等．

关键词： 小数乘法 位宽 缺省 逻辑单元 功耗

Optimization methodology for the width of the fixed-point decimal multiplier

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Abstract:

With the progress of design and fabrication in the semiconductor area, the chip scale and complexity are raised rapidly, and low-power design becomes a very important topic. This paper presents a low-power optimization methodology for the width of the fixed-point decimal multiplier, describes its principle and implementation, and verifies its optimization result by the FPGA test. On the methodological level, its optimization object is the width of the adders, which are inside the synthesized multiplier. On the circuit level, it resolves the problem of introducing the logic in the optimized system, which exists in the present low power design. The methodology has good performance in optimizing the system including large-scale multipliers, such as DSP, digital filter, etc.

Keywords: decimal multiplication   data width   omit   logic cell   power

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