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研究论文

针对乘法器内部加法运算次数的优化算法

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摘要：

提出一种针对乘法器的低功耗设计算法，其优化指标为乘法器内部加法运算次数．在实现技术上，解决了目前低功耗设计中算法自身逻辑单元被引入系统从而降低系统优化效果的问题．该算法能够在不降低系统工作效率、不损失系统运算精度、不增加额外逻辑单元的条件下，大幅降低系统功耗和面积．在使用该算法对某一射频模块进行优化后，硬件测试结果显示该射频模块对某型号FPGA的逻辑占用率相比优化前降低32.1%，寄存器总数降低33.1%，存储单元占用率降低35.4%，优化效果显著．

关键词： 乘法系数 加法运算数量 优化逻辑单元 功耗分析

Optimization methodology for the number of additions in multiplier

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Abstract:

This paper presents a low-power design methodology for the multiplier, whose optimization specification is the number of operations of the adders inside synthesized multiplier. The implementation technique resolves the problem of the optimization logic being introduced into the optimized system, which exists in present low power design. It can reduce system power and area significantly without an additional logic, a declined system working efficiency and a declined calculation accuracy. After a radio-frequency circuit is optimized, FPGA test results show that logic utilization is reduced by 32.1%, total registers number is reduced by 33.1%, and total block memory bits utilization is reduced by 35.4%. The methodology has good performance in optimizing the system including large-scale multipliers, such as DSP, digital filter, etc.

Keywords: coefficient of multiplier number of addition optimization logic power analysis

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参考文献：

［1］ 邓军, 杨银堂. 全数字接收机中一种低功耗插值滤波器结构及其VLSI实现［J］. 西安电子科技大学学报, 2010, 37(2) 320-325.
Deng Jun, Yang Yintang. The VLSI Implementation of a Low-power Interpolation Filter Structure in All-digital Receiver ［J］. Journal of Xidian University, 2010, 37(2): 320-325.
［2］ 何学辉, 吴兆平, 苏涛, 等. 任意相位编码信号及其脉压滤波器联合优化设计［J］. 西安电子科技大学学报, 2009, 36(6): 1027-1033.
He Xuehui, Wu Zhaoping, Su Tao, et al. Joint Optimization Design of Any Phase-encoded Signal and the Pulse Pressure Filter ［J］. Journal of Xidian University, 2009, 36(6): 1027-1033.
［3］ 蒋俊正, 王小龙, 水鹏朗. 一种设计DFT调制滤波器组的新算法［J］. 西安电子科技大学学报, 2010, 37(4):

689-693.
Jiang Junzheng, Wang Xiaolong, Shui Penglang. A New Algorithm of DFT Modulated Filter［J］. Journal of Xidian University, 2010, 37(4): 689-693.
［4］ Kodi A K, Sarathy A, Louri a, et al. Adaptive Inter Router Links for Low Power, Area Efficient and Reliable Network on Chip (NoC) Architectures［C］//ASP2DAC 2009. Athens: Ohio Univ, 2009: 1-126.
［5］ Kodi A, Louri A, Wang J. Design of Energy Efficient Channel Buffers with Router Bypassing for Network on Chips (NoCs) ［M］. San Jose: Quality of Electronic Design, 2009: 826-832.
［6］ Wong A C W, Kathiresan G. A 1V Wireless Transceiver for an Ultra Low Power SoC for Biotelemetry Applications［C］//European Solid State Circuits Conf. Abingdon: Toumaz Technol Ltd, 2007: 127-130.
［7］ Daniele L, Macro R. Binary Canonic Signed Digit Multiplier for High-speed Digital Signal Processing［C］//The 2004 47th Midwest Symposium on Circuits and Systems. Hiroshima: ［s.n.］, 2004: 33-68.
［8］ Graillat S, Langlois P, Louvet N. Compensated Horner Scheme［C］//Technical Report. Perpignan: University of Perpignan, 2005: 10-26.
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