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个人简介
个人主页

安丰伟博士于2019年加入南方科技大学，任副教授。安丰伟博士的主要研究领域是基于计算机视觉的低功耗边缘人工智能芯片设计，具体包括图像处理、图像识别、机器学习的超大规模数字集成电路设计和系统集成，并有在工业界的研究开发经验。

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教育经历
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代表文章

.1. Journal paper
Guan, J., An, F., Zhang, X., Chen, L.,Mattausch, H. J., Energy-Efficient Hardware Implementation of Road-Lane Detection Based on Hough Transform with Parallelized Voting Procedure and Local Maximum Algorithm, IEICE Transaction on information systems, 2019.
Luo, A.& An, F. & Zhang, X. & Mattausch, H.J., (2019). A Hardware-Efficient Recognition Accelerator Using Haar-Like Feature and SVM Classifier. IEEE Access. PP. 1-1. 10.1109/ACCESS.2019.2894169.
An, F., Zhang, X., Luo, A., Chen, L., & Mattausch, H. J. , A Hardware Architecture for Cell-based Feature-Extraction and Classification Using Dual-Feature Space, IEEE Transactions on Circuits and Systems for Video Technology (TCSVT), DOI: 10.1109/TCSV2017.2726564, Jul. 13, 2017.
Zhang, X., An, F., Chen, L., Ishii, I., & Mattausch, H. J., A Modular and Reconfigurable Pipeline Architecture for Learning Vector Quantization,IEEE transaction on circuits and system I: Regular papers (TCAS I), DOI: 10.1109/TCSI.2018.2804946, Feb. 23, 2018.
Huang, Z., Zhang, X., Chen, L., Zhu, Y., An, F.*, Wang, H., & Feng, S., A Vector-Quantization Compression Circuit with On-Chip Learning Ability for High-Speed Image Sensor, IEEE Access, 5, 22132-22143, Oct. 17, 2017.
Guan, J., An, F., Zhang, X., Chen, L., & Mattausch, H. J., (2017), Real-Time Straight-Line Detection for XGA-Size Videos by Hough Transform with Parallelized Voting Procedures, Sensors, 17(2), 270, Jan. 30, 2017.
Huang, Z.,Suzuki, D., Zhang, X., Chen, L., Zhu, Y., An, F., Wang, H., Feng, S., J. Mattausch, (2019). A Hardware-Efficient Vector Quantizer Based on Self-Organizing Map for High-Speed Image Compression. Appl. Sci. 2017, 7, 1106. Applied Sciences. 9. 1377. 10.3390/app9071377.
Luo, A., An, F., Zhang, X., Chen, L., & Mattausch, H. J., Resource-Efficient Object-Recognition Coprocessor with Parallel Processing of Multiple Scan Windows in 65-nm CMOS, IEEE Transactions on Very Large Scale Integration (VLSI) Systems (TVLSI), 26(3), 431-444, Dec. 04, 2017.
F.An, X. Zhang, L. Chen, and H.J. Mattausch, A Memory-based Modular Architecture for SOM and LVQ with Dynamic Configuration, IEEE Transactions on Multi-Scale Computing Systems (TMSCS), Vol.2 (4), pp. 234-241, 2016.
Luo, A., An, F., Zhang, X., Chen, L., Huang, Z., Mattausch, H.J., (2018), Flexible feature-space-construction architecture and its VLSI implementation for multi-scale object detection, Japanese Journal of Applied Physics, 57(4S), 04FF04, Mar. 02, 2018.
Zhang, X., An, F., Nakashima, I., Luo, A., Chen, L., Ishii, I., & Mattausch, H. J., A hardware-oriented histogram of oriented gradients algorithm and its VLSI implementation, Japanese Journal of Applied Physics, 56(4S), 04CF01, Jan. 30, 2017.
Luo, A., An, F., Fujita, Y., Zhang, X., Chen, L., & Mattausch, H. J., (2017), Low-power coprocessor for Haar-like feature extraction with pixel-based pipelined architecture, Japanese Journal of Applied Physics, 56(4S), 04CF06, Mar. 07, 2017.
An, F., K. Mihara, S. Yamasaki, L. Chen, and Mattausch, K-Nearest Neighbor Associative Memory with Reconfigurable Word-Parallel Architecture, Journal of Semiconductor Technology and Science, 16(4):405-414, Aug. 2016.
An, F., K. Mihara, S. Yamasaki, L. Chen, and Mattausch, Highly flexible nearest-neighbor-search associative memory with integrated k nearest neighbor classifier, configurable parallelism and dual-storage space, Japanese Journal of Applied Physics, 55(4S):04EF10, April 2016.
Zhang, An, F., L. Chen, and H.J. Mattausch, Reconfigurable VLSI implementation for learning vector quantization with on-chip learning circuit,Japanese Journal of Applied Physics, 55(4S):04EF02 April 2016.
An, F., L. Chen, T. Akazawa, and H.J. Mattausch, k Nearest Neighbor Classification Coprocessor with Weighted Clock-Mapping-Based Searching, IEICE Transactions on Electronics, E99.C (3):397-403, March 2016.
An, F., T. Akazawa, S. Yamasaki, L. Chen, and H. J. Mattausch, VLSI realization of learning vector quantization with hardware/software co-design for different applications. Japanese Journal of Applied Physics, vol.54, no.4s, pp. 4DE05, 2015.
An, F. and H. J. Mattausch, K-means Clustering Algorithm for Multimedia Applications with Flexible HW/SW Co-design, Journal of System Architecture, (59), pp.155-164, 2013.
I.Wicaksono, F. An, and H.J. Mattausch, Memory Based Hardware-Accelerated System for High-Speed Human Recognition, Advanced Robotics, 28 (5), pp.317-327, 2014.
F.An, T. Koide, and H. J. Mattausch, A K-means-based Multi-Prototype High-Speed Learning System with FPGA-implemented Coprocessor for 1-NN Searching, IEICE Transaction on information systems, Vol. E95-D, No.9, 2327-2338, 2012.
.Selected Conference papers
An, F., Multi-port SRAM with Multi-bank for Self-organizing Maps Neural Network, IEEE International Conference on Solid-state and Integrated Circuit Technology, Oct. 2018. (Invited)
An, F., Zhang, X., Chen, L. & Ishii, I., Object-recognition VLSI for pedestrian detection in automotive applications. In IEEE 12th International Conference on ASIC (ASICON), China, Guiyang, Oct., pp. 651-653. 2017. (Invited)
An, F., Zhang, X., Chen, L., & Mattausch, H. J., "Dynamically Reconfigurable System for LVQ-based On-Chip Learning and Recognition," In IEEE International Symposium on Circuits and Systems (ISCAS), Canada, Montreal, May, pp. 1338-1341, 2016.
An, F., X. Zhang, L. Chen, and H.J. Mattausch, Parallel-Elementary-Stream Architecture for Nearest-Neighbor-Search-based Self-Organizing Map, IEEE International Conference on Solid-state and Integrated Circuit Technology, Oct. 2016. (Invited)
.Pang, H. Huang, An, F., and H. Yu, Low-power and Real-time Computer Vision On-chip, in13thIEEE International SoC design Conference, South Korea, Jeju, Oct. 2016. (Invited)
An, F., T. Akazawa, S. Yamasaki, L. Chen, and H. J. Mattausch, Word-parallel Associative Memory for k-Nearest-Neighbor with Configurable Storage Space of Reference Vectors, IEEE Asian Solid-State Circuits Conference (ASSCC), China, Xiamen, pp. 1-4, 2015.
An, F., T. Akazawa, S. Yamazaki, L. Chen, and H.J. Mattausch, A Coprocessor for Nearest Clock-based Euclidean Distance Search towards multiple applications, IEEE Custom Integrated Circuits Conference (CICC), USA, California, pp. 1-6, 2014.
.3. Issued Patent
An, F., Mattausch, H. J., Chen, L., Zhang, X., & Luo, A.,Image recognition device, Application No: JP2017-030253.

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