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高精度S-DADC中的数字抽取滤波器设计

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摘 要：设计1个应用于高精度sigma-delta模数转换器(S-DADC)的数字抽取滤波器。数字抽取滤波器采用0.35 mm工艺实现，工作电压为5 V。该滤波器采用多级结构，由级联梳状滤波器、补偿滤波器和窄带有限冲击响应半带滤波器组成。通过对各级滤波器的结构、阶数以及系数进行优化设计，有效地缩小了电路面积，降低了滤波器的功耗。所设计的数字抽取滤波器通带频率为21.77 kHz，通带波纹系数为±0.01 dB，阻带增益衰减120 dB。研究结果表明：该滤波器对128倍过采样、二阶S-D调制器的输出码流进行处理，得到的信噪失真比达102.8 dB，数字抽取滤波器功耗仅为49 mW，面积约为0.6 mm×1.9 mm，达到了高精度模数转换器的要求。

关键字：S-DADC模数转换器；调制器；降采样；数字滤波器

Design of digital decimation filter for high resolution S-DADC

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Abstract:A multistage digital decimation filter for high resolution sigma-delta analog-to-digital converter (S-DADC) was designed. The filter was fabricated by a 0.35 mm process and operates at a voltage of 5 V. The filter consists of a cascade-integrator-comb (CIC) filter, a compensation filter and narrow transition-band finite impulse response (FIR) half-band filter. Due to the optimal design of the architecture and order and coefficient of filters at various levels, the decimation filter effectively reduces the circuit area and power dissipation. The decimation filter has pass band of 21.77 kHz, pass band ripple coefficient of ±0.01 dB and stopped band attenuation of 120 dB. Experimental results show that by processing the bit stream from a 2-order Σ-Δ modulator with an oversampling ratio of 128, a signal-to-noise-distortion ratio (SNDR) of 102.8 dB is obtained for the filter. The filter has a good performance and its dissipation powder is only 49 mW. The occupied die area is about 0.6 mm×1.9 mm. The filter well meets the demand of high resolution S-DADC.

Key words:S-DADC analog-to-digital converter; modulator; decimation; digital filter

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