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软件、算法与仿真

一种异构多核片上系统的SystemC系统级综合方法

针对传统集成电路综合方法的不足，提出了一种异构多核片上系统的SystemC系统级综合方法。阐述了系统级综合的SystemC非定时设计输入模型，给出了多核控制器做复杂控制和算法IP做运算加速的目标片上系统架构及综合流程。在此基础上开发了SystemC系统级综合集成开发环境，并进行了通信处理异构多核片上系统的设计和实现。实验结果表明，该方法有效地提高了软硬件混合片上系统的设计效率， 缩短了研制周期。

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摘要：

针对传统集成电路综合方法的不足，提出了一种异构多核片上系统的SystemC系统级综合方法。阐述了系统级综合的SystemC非定时设计输入模型，给出了多核控制器做复杂控制和算法IP做运算加速的目标片上系统架构及综合流程。在此基础上开发了SystemC系统级综合集成开发环境，并进行了通信处理异构多核片上系统的设计和实现。实验结果表明，该方法有效地提高了软硬件混合片上系统的设计效率, 缩短了研制周期。

关键词： 大规模集成电路 SystemC 系统级综合 体系结构

SystemC system level synthesis method for heterogeneous MPSoC

Aiming at the shortcoming of the traditional large scale integrated circuit synthesis method, a novel SystemC electronic system level synthesis (SLS) method is proposed. The heterogeneous multiprocessor system on a chip (MPSoC) hardware architecture which is the target for a system level synthesis system and a SLS synthesis flow are described. The SLS method supports a SystemC untimed model as its design entry and adopts the target MPSoC hardware architecture that has a multiprocessor as the controller and algorithmic IPs as computation accelerators. Furthermore, a system level synthesis integrated development environment (IDE) is implemented, and a MPSoC processor is developed with the IDE. Experimental results show that the proposed synthesis method improves the efficiency of software/hardware mixed MPSoC systems effectively and reduces the time put on the market.

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Abstract:

Aiming at the shortcoming of the traditional large scale integrated circuit synthesis method, a novel SystemC electronic system level synthesis (SLS) method is proposed. The heterogeneous multiprocessor system on a chip (MPSoC) hardware architecture which is the target for a system level synthesis system and a SLS synthesis flow are described. The SLS method supports a SystemC untimed model as its design entry and adopts the target MPSoC hardware architecture that has a multiprocessor as the controller and algorithmic IPs as computation accelerators. Furthermore, a system level synthesis integrated development environment (IDE) is implemented, and a MPSoC processor is developed with the IDE. Experimental results show that the proposed synthesis method improves the efficiency of software/hardware mixed MPSoC systems effectively and reduces the time put on the market.

Keywords: large scale integrated circuit SystemC system level synthesis (SLS) architecture

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