

应用

基于一种交织码的多位翻转容错技术研究

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摘要:

随着技术的发展和核心电压的降低,存储器更易受瞬时错误(软错误)影响,成为影响航天器件可靠性的主要原因。错误检测与纠正(EDAC)码(也称错误纠正码)常用来对SRAM型存储器中的瞬时错误进行纠正,由单个高能粒子引起的多位翻转错误(SEMU)是普通纠一检二(SEC-DED)编码所无法处理的。提出了一种交织度为2的(26,16)交织码,该码由两个能纠正一位随机错误、二位突发错误的(13,8)系统码组成,(26,16)交织码能够纠正单个码字中小于二位的随机错误和小于四位突发错误(DEC-QAEC)。通过理论分析和硬件平台实验表明,该交织码在存储资源占用率、实时性相当情况下可靠性优于同等长度的SEC DED码,能有效提高SRAM型存储器抗多位翻转错误的能力。

关键词: 静态存储器; 错误纠正码; 单字节多位翻转; 随机错误; 突发错误

Study of the Multiple Bit Upset Tolerant Technology Base on a Interlaced Code

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Abstract:

As technology scales and the supply voltage decreases, memories are becoming more prone to transient errors (also called soft errors). Thus memories are the major causes of reliability problems in modern integrated circuits. Error detect and correct codes (also called error correct codes) have been well-known used to correct transient errors in SRAMs memory, a single high-energy particle affects several adjacent memory cells upsets (Single Event Multi-Bit Upset), could not be corrected by single error correcting codes, such as Single-Error-Correcting Double-Error-Detecting(SEC-DED) code. A (26, 16) interlaced code was proposed for less than two random errors correction, less than quadruple adjacent error correction (DEC-QAEC), which was composed by two systematic (13, 8) codes for correcting single errors and adjacent two errors. Theoretic analysis and simulation results show that the interlaced code is better than SED-DED code of the same length on the reliability under the equivalent memory overhead and the real-time performance. The reliability of SRAMs can be obviously improved protected against the multi-bit upset with the proposed code.

Keywords: burst errors

收稿日期 2011-12-16 修回日期 2012-04-10 网络版发布日期 2012-06-25

DOI:

基金项目:

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