

论文

并行BCH伴随式计算电路的优化

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摘要:

随着通信系统的速率越来越高, 对BCH译码器吞吐量的要求也不断提高。由于BCH码是串行的处理数据, 在吞吐量大的应用时一般需要并行处理, 但这会导致电路的复杂度显著增加。本文主要研究并行伴随式计算电路的优化。通过合并输入端的常量乘法器, 得到改进的并行伴随式结构。该结构克服了传统方法只能对局部的乘法器进行优化的缺点, 可以对全部乘法器进行优化, 从而有效的减少逻辑资源。实验结果表明, 对于并行度为64的BCH(2040, 1952)译码器, 本文的优化结构可以节省67%的逻辑资源, 而且在并行度、纠错能力和码长变化时, 仍然可以获得较好的优化结果。

关键词: 伴随式计算电路 并行处理 BCH码

Optimization of parallel syndrome computation for BCH codes

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Abstract:

Due to the increasing demand for high capacity of communications, Bose-Chaudhuri-Hochquenghem decoders with high throughput are desirable to meet higher data rate. Since the BCH codes conduct the bit-by-bit error correction, they often need a parallel implementation for high throughput application. In this paper, we propose the optimization for the parallel syndrome computation architecture. The improved architecture is proposed by simplifying the multipliers of the input. In the improved architecture, all the multipliers can be optimized, while only part of the multiplier can be optimized by the traditional methods. The experimental results show that the hardware complexity can be reduced by 67% in the design of the BCH(2040, 1952) codes with parallel factor 64. In different cases of parallel factors, error correcting capability and codeword length, the improved architecture also have good performance compared with the traditional methods.

Keywords: Bose-Chaudhuri-Hochquenghem (BCH) codes; parallel processing; syndrome computation

收稿日期 2009-06-15 修回日期 网络版发布日期 2010-03-25

DOI:

基金项目:

通讯作者:

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