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A Theoretical Approach to Fault Analysis and Mitigation in Nanoscale Fabrics

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Abstract
High defect rates are associated with novel nanodevice-based systems owing to unconventional and self-assembly based manufacturing processes. Furthermore, in emerging nanosystems, fault mechanisms and distributions may be very different from CMOS due to unique physical layer aspects, and emerging circuit and logic styles. Thus, theoretical fault models for nanosystems are necessary to extract detailed characteristics of fault generation and propagation. Using the intuition garnered from the theoretical analysis, modular and structural redundancy schemes can be specifically tailored to the intricacies of the fabric in order to achieve higher reliability of output signals.

In this thesis, we develop a detailed analytical fault model for the Nanoscale Application Specific Integrated Circuits (NASIC) fabric that can determine probabilities of output faults taking into account the defect scenarios, the logic and circuit style of the fabric as well as structural

redundancy schemes that may be incorporated in the circuits. Evaluation of fault rates using the analytical model for single NASIC tiles show an inequality of the probability of output faulty ‘1’s and ‘0’s. To mitigate the effects of the unequal fault rates, biased voting schemes are introduced and are shown to achieve up to 27% improvement in the reliability of output signals compared to conventional majority voting schemes.

NASIC circuits have to be cascaded in order to build larger systems. Furthermore, modular redundancy alone will be insufficient to tolerate high defect rates since multiple input modules may be faulty. Hence incorporation of structural redundancy is crucial. Thus in this thesis, we study the propagation of faults through a cascade of NASIC circuits employing the conventional structural redundancy scheme which is referred to here as the *Regular Structural Redundancy*. In our analysis we find that although circuits with *Regular Structural Redundancy* achieve greater signal reliability compared to non-redundant circuits, the signal reliability rapidly drops along the cascade due to an escalation of faulty ‘0’s. This effect is attributed to the poor tolerance of input faulty ‘0’s exhibited by circuits with the Regular Structural Redundancy. Having identified this, we design a new scheme called the *Staggered Structural Redundancy* prioritizing the tolerance of input faulty ‘0’s. A cascade of circuits employing the *Staggered Structural Redundancy* is shown to maintain signal reliability greater than 0.98 for over 100 levels of cascade at 5% defect rate whereas the signal reliability for a cascade of circuits with the Regular Structural Redundancy dropped to 0.5 after 7 levels of cascade.

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