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Testable Clock Distributions for 3D Integrated Circuits

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Abstract

The 3D integration of dies promises to address the problem of increased die size caused by the slowing of scaling. By partitioning a design among two or more dies and stacking them vertically, the average interconnect length is greatly decreased and thus power is reduced. Also, since smaller dies will have a higher yield, 3D integration will reduce manufacturing costs. However, this increase in yield can only be seen if manufactured dies can be tested before they are stacked. If not, the overall yield for the die stack will be worse than that of the single, larger die.

One of the largest issues with prebond die testing is that, to save power, a single die may not have a complete clock distribution network until bonding. This thesis addresses the problem of prebond die testability by ensuring the clock distribution network on a single die will operate with low skew during testing and at a reduced power consumption during operation as compared to a full clock network. The development of a Delay Lock Loop is detailed and used to synchronize disconnected clock

networks on a prebond die. This succeeds in providing a test clock network that operates with a skew that is sufficiently close to the target postbond skew.

Additionally, a scheme to increase interdie bandwidth by multiplexing Through-Silicon Vias (TSVs) by the system clock is presented. This technique allows for great increase in the number of effective signal TSVs while imposing a negligible area overhead causing no performance degradation.

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