研究简报

一种针对AVS去块滤波的高性能结构

方 健①, 凌 波②, 王 匡②

①浙江大学城市学院 杭州 310015; ②浙江大学信息与电子工程学系 杭州 310027

摘要
在AVS视频解码器设计中，环路去块滤波成为实时处理的瓶颈之一。该文提出了一种实用的环路滤波结构，处理一个宏块只需要164个周期。使用新颖的滤波顺序，待滤波数据缓冲从16×16宏块大小降低为16×8半宏块大小。使用数据重用策略，滤波中间数据的存储空间大大减小。实验表明，使用0.18μm CMOS工艺，在50MHz下综合，该文提出的设计只需要9.2k门。工作在50MHz频率下，该文提出的设计能够支持高清视频解码的实时滤波处理。

关键词　视频编码　去块滤波　硬件结构

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High-Performance Architecture of Deblocking Filter for AVS Video Coding

Fang Jian①, Ling Bo②, Wang Kuang②

①Zhejiang University City College, Hangzhou 310015, China; ②Department of Information Science and Electronic Engineering, Zhejiang University, Hangzhou 310027, China

Abstract
In the video decoder for AVS, deblocking filter becomes one of the bottom necks for real-time processing. An implement architecture for deblocking filter is proposed in this paper. With a novel filtering order, the unfiltered data storage is reduced to a 16×8 block instead of whole 16×16 macroblock。With data reuse strategy, the intermediate data storage is also reduced efficiently. The experiment shows the proposed design can achieve 50 MHz with only gate count of 9.2k by using 0.18μm CMOS technology. When clocked at 50MHz, the proposed design can support real-time deblocking of HD1080 (1980×1088@30Hz) video application.

Key words　Video coding　Deblocking filter　Hardware architecture

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作者个人主页　　方 健①; 凌 波②; 王 匡②