



基于全双工以太帧间隔的源同步时钟传输方法

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Source Synchronized Clock Transmission Based on Inter-Packet Gap of Full-Duplex Ethernet

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摘要

提出在全双工以太物理层中, 基于以太帧间隔 (inter packet gap, IPG) 的固定比特率业务同步时钟传输方法. 该方法引入同步剩余时戳(synchronous residual time stamp, SRTS)算法, 是一种不受以太分组流量影响的带外时钟传输方法. 通过连分数展开分析恢复时钟的各阶抖动成分, 给出基于以太帧间隔的同步剩余时戳算法的参数选择方法, 并通过软件仿真和现场可编程门阵列(field programmable gate array, FPGA)硬件实验证明了其优良的同步性能.

关键词: [帧间隔](#); [同步剩余时戳](#); [源时钟同步](#)

Abstract:

A source synchronized clock transmission method is proposed based on inter-packet gap (IPG) of Ethernet running in a full-duplex mode. A synchronous residual time stamp (SRTS) is adopted as the clock transmission algorithm. The characteristic of the new method is immune to fluctuation for in-band Ethernet traffic. Parameters of the SRTS algorithm used in Ethernet IPG and the output jitter waveform of recovered clock are determined by using continued fraction. Simulation results and field programmable gate array (FPGA) implementation are given to demonstrate high quality of the recovered clock.

Keywords: [inter-packet gap \(IPG\)](#); [synchronous residual time stamp \(SRTS\)](#); [source clock synchronization](#)

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