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基于单驱动和多驱动通道形式组合的FPGA互连结构研究

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Optimal Design for FPGA Interconnect Based on Combinations of Single-driver and Multi-driver Wires

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摘要

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摘要 单驱动实现和多驱动实现是FPGA中单向互连通道的两种实现形式。该文讨论了二者在版图面积、延时等方面的差异,以及它们各自对通道结构的限制。提出在互连结构中将两种实现形式进行组合。并给出一种有效的结构设计方法,通过两级优化得到了面积延时积最优情况下对应的互连线段长度组合方式以及互连实现形式组合方式。与其他结构相比,使用该文方法得到的50%长度为6的单驱动电路,25%长度为8的多驱动电路和25%长度为8的单驱动电路的组合结构,改进了57%~86%的面积延时积。

关键词: FPGA 互连结构 单驱动实现 多驱动实现 面积延时积

Abstract: Single-driver directional wires and multi-driver directional wires can both be used for FPGA interconnect. This paper compares them in area, performance, and their effect on topology of the routing architecture. Then a new type of FPGA routing architecture is proposed that utilizes a mixture of single-driver and multi-driver wires combined with various wire lengths and a two-stage optimization method is used to obtain the best routing architecture. Extensive experiments show that the best architecture optimized by area-delay product is 50% length 6 wires with single-driver, 25% length 8 wires with multi-driver and 25% length 8 wires with single-driver. This results in FPGA with $57\% \sim 86\%$ gain in area-delay product.

Keywords: FPGA Interconnect Single-driver Multi-driver Area-delay product

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