文 章 内 容

标　题：	Adaptive explicitly parallel instruction computing for embedded systems
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发表年限：	2003
发表期号：	6
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关键词：	adaptive EPIC ； instruction synthesis；dynamic reconfiguration
摘　要：	Reconfigurable hardware offers the embedded system s the potential for significant performance improvements by providing support for application—specific operations． Adaptive Explicitly Parallel Instruction Computing is a prototype model such that fine—grain and dynamically reconfigurable structure is tightly coupled with a generic EPIC machine． AEPIC allows application program s to add specialized functional units yielding a dynamically varying instruction set interface to the running application without compromising current compatibility mode1． Two advantages of AEPIC are① dynamic configuration support；③application specific instruction set synthesis． In order to investigate the idea of AEPIC s potential realistic experiments are conducted in an environment that incorporates the A EPIC simulator and actual reconfigurable hardware of Xilinx FPGA． Results show that AEPIC can achieve the similar or higher perform —ance at a much lower execution frequency，com pared with EPIC．  Adaptive expl icitl y paral l el instruction com puting.pdf

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