# Turkish Journal of Electrical Engineering & Computer Sciences

## Four quadrant FGMOS analog multiplier

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**Abstract:** A novel four-quadrant analog multiplier using floating gate MOS (FGMOS) transistors operating in the saturation region is presented. The drain current is proportional to the square of the weighted sum of the input signals. This square law characteristic of the FGMOS transistor is used to implement the quarter square identity by utilizing only six FGMOS transistors. The main features of this remarkably simple multiplier circuit configuration are the large input signal range equal to 100% of the supply voltage, nonlinearity of 0.0081%, bandwidth of 1.4--1.5 Ghz and THD of maximum 2.67% (while the inputs are at their maximum values).

**Key words:** FGMOS, four quadrant analog multiplier, rail-to-rail, differential amplifier