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Two-Dimensional Stack Generation and Block Merging Algorithms for Analog VLSI

LIU Rui, DONG She-Qin, HONG Xian-Long, LONG Di, GU Jun

LIU Rui1,2, DONG She-Qin2, HONG Xian-Long2, LONG Di2, GU Jun3, 1(Institute of Software, The Chinese Academy of Sciences, Beijing 100080, China)2(Department of Computer Science and Technology, Tsinghua University, Beijing 100084, China)3(Department of Computer Science, Science and Technology University of Hong Kong, Hong Kong, China)
Authors information: LIU Rui was born in 1974. He is a Ph.D. candidate at the Institute of Software, Chinese Academy of Sciences. His research areas are algorithm and analog VLSI CAD. DONG She-Qin was born in 1964. He is an associate professor at the Department of Computer Science and Technology, Tsinghua University. His research areas are optimization algorithm and VLSI physical design. Hong Xian-Long was born in 1940. He is a professor and doctoral supervisor at the Department of Computer Science and Technology, Tsinghua University. His research areas are algorithm and CAD system. LONG Di was born in 1980. He is PhD candidate at the Department of Computer Science and Technology, Tsinghua University. His research interests focus on analog layout automation. GU Jun is with the Department of Electrical and Computer Engineering, University of Calgary, Alberta T2N 1N4, Canada, and is visiting the Department of Computer Science, Hong Kong University of Science and Technology, Hong Kong, China. His research areas are SAT problem, optimization algorithm and VLSI CAD.
Corresponding author: LIU Rui, E-mail: rliu_ac@hotmail.com, http://www.iscas.ac.cn
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Abstract
In analog VLSI design, 2-dimensional symmetry stack and block merging are critical for mismatch minimization and parasitic control. In this paper, algorithms for analog VLSI 2-dimensional symmetry stack and block merging are described. Several theoretical results are obtained by studying symmetric Eulerian graph and symmetric Eulerian trail. Based on them, an O(n) algorithm for dummy transistor insertion, symmetric Eulerian trail construction and 2-dimensional symmetry stack construction is developed. The generated stacks are 2-dimensional symmetric and common-centroid. A block merging algorithm is described, which is essentially independent of the topological representation. Formula for calculating the maximum block merging distance is given. Experimental results show the effectiveness of the algorithms.

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摘要
在模拟集成电路设计中,关于X轴和Y轴同时对称的Stack,以及模块之间的合并,对于增加器件之间的匹配和控制寄生是至关重要的.描述了模拟集成电路二轴对称Stack生成算法和模块合并算法.通过对于对称欧拉图和对称欧拉路径的研究,得出了多项理论结果.在此基础上,提出了时间复杂度为O(n)的伪器件插入算法、对称欧拉路径构造算法和二轴对称Stack生成算法.生成的Stack,不但关于X轴和Y轴对称,而且具有公共质心(common- centroid)的结构.还描述了模块合并算法,给出了计算最大合并距离的公式.该算法本质上是独立于任何拓扑表示的.实验结果验证了算法的有效性.

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