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Towards Logic Functions as the Device using Spin Wave Functions Nanofabric

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Abstract
As CMOS technology scaling is fast approaching its fundamental limits, several new nano-electronic devices have been proposed as possible alternatives to MOSFETs. Research on emerging devices mainly focusses on improving the intrinsic characteristics of these single devices keeping the overall integration approach fairly conventional. However, due to high logic complexity and wiring requirements, the overall system-level power,

performance and area do not scale proportional to that of individual devices.

Thereby, we propose a fundamental shift in mindset, to make the devices themselves more functional than simple switches. Our goal in this thesis is to develop a new nanoscale fabric paradigm that enables realization of arbitrary logic functions (with high fan-in/fan-out) more efficiently. We leverage on non-equilibrium spin wave physical phenomenon and wave interference to realize these elementary functions called *Spin Wave Functions (SPWFs)*.

In the proposed fabric, computation is based on the principle of wave superposition. Information is encoded both in the phase and amplitude of spin waves; thereby providing an opportunity for compressed data representation. Moreover, spin wave propagation does not involve any physical movement of charge particles. This provides a fundamental advantage over conventional charge based electronics and opens new horizons for novel nano-scale architectures.

We show several variants of the SPWFs based on topology, signal weights, control inputs and wave frequencies. SPWF based designs of arithmetic circuits like adders and parallel counters are presented. Our efforts towards developing new architectures using SPWFs places strong emphasis on integrated fabric-circuit exploration methodology. With different topologies and circuit styles we have explored how capabilities at individual fabric components level can affect design and vice versa. Our estimates on benefits vs. 45nm CMOS implementation show that, for a 1-bit adder, up to 40x reduction in area and 228x reduction in power is possible. For the 2-bit adder, results show that up to 33x area reduction and 222x reduction in power may be possible.

Building large scale SPWF-based systems, requires mechanisms for synchronization and data streaming. In this thesis, we present data streaming approaches based on Asynchronous SPWFs (A-SPWFs). As an example, a 32-bit Carry Completion Sensing Adder (CCSA) is shown based on the A-SPWF approach with preliminary power, performance and area evaluations.

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