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A Parallel Pipelined Computer Architecture for Digital Signal Processing

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Abstract: This paper presents a parallel pipelined computer architecture and its six network configurations targeted for the implementation of a wide range of digital signal processing (DSP) algorithms described by both atomic and large grain data flow graphs. The proposed architecture is considered together with programmability, yielding a system solution that combines extensive concurrency with simple programming. It is an SSIMD (Skewed Single Instruction Multiple Data) or MIMD (Multiple Instruction Multiple Data) machine depending on the algorithms implemented and the programming methodologies. The concurrency that can be exploited by the algorithms using this Parallel pipelined architecture is both temporal and spatial concurrency. The third level of concurrency (second spatial concurrency) can be also achieved by using input and output synchronized circular buses. An experimental parallel pipelined AdEPar (Advanced Educational Parallel) DSP system architecture, and its network configurations using printed circuit boards (as processing elements-PEs) based on DSP processors were designed and implemented. The hardware debugging of parallel programs and development of other high level programming tools such as automatic task schedulers and code generators) are relatively easy for the AdEPar architecture compared with other architectures having complicated interprocessor communications. Keywords: Digital signal processing, parallel processing, parallel pipelined architecture.

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