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博士论坛

一种实现高速异步FIFO的FPGA方法

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摘要 在跨时钟域传递数据的系统中，常采用异步FIFO（First In First Out，先进先出队列）口来缓冲传输的数据，以克服亚稳态产生的错误，保证数据的正确传输。但由于常规异步FIFO模块中的RAM存储器读写寻址指针常采用格雷码计数器以及“空满”控制逻辑的存在，将使通过这两个模块的信号通路延时对整个模块的工作频率造成制约。提出了一种在FPGA内实现高速异步FIFO的方法，该方法针对不可能产生满信号的高频系统，通过省略“满”信号产生模块和多余的存储器位深来简化常规的FIFO模块，而只保留“空”信号产生模块。仿真和综合设计结果表明，整个模块的工作频率得到一定提高。

关键词 现场可编程门阵列（FPGA） 亚稳态 格雷码 高速FIFO

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Implementation method of high-speed asynchronous FIFO using FPGA

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Abstract

To overcome the metastability and ensure the validation of data transfer，the asynchronous First In First Out（FIFO）modules are often used to buffer data in systems with data transfers crossing clock domains.Because of the existence of the addressing pointers，which often adopt Gray-code counters，and the“full & empty” generation logic in a usual asynchronous FIFO module，the signals passing two modules may suffer large delay.As a result，the working frequency of the whole module is limited.Based on a premise that the“full” state will never occur in a high-frequency system，a method of implementing high speed asynchronous FIFO in FPGA is proposed.The focus on this way is that the “full” flag generation logic and redundant RAM depth are omitted，i.e.，only the“empty” flag is generated.So，the design of FIFO is simplified.The results from simulation and synthesis design show that the working speed of the whole module is greatly increased.

Key words Field-Programmable Gate Array（FPGA） metastability gray-code high-speed FIFO

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