Title

A Framework for High Level Synthesis Using Taylor Decomosition System

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Abstract

This thesis extends the work and application of Taylor Expansion Diagrams (TED) as a framework for high level synthesis and verification of data-flow and arithmetic-intensive designs. It shows that TEDs can be used for different high level optimization objectives and that TED-based optimizations and transformations translate into actual gains in hardware. The first metric it tackles is area and latency optimization. This optimization has been studied in previous works, but reported gains were marginal and not driven by actual hardware performance. Specifically, the previously used metrics for decomposition targeted the minimization of the number of operations in the arithmetic data-path, assuming that this optimization would translate into latency or area gains. We show that such minimization does not produce noticeable hardware gains in terms of resource utilization or performance. We demonstrate that we can obtain more efficient hardware implementations with other decomposition methods which directly address those tangible hardware metrics. In this manner we demonstrate that TED is a valid framework for area and latency optimization and put a closure on this subject. Furthermore, we propose an extension to Taylor Expansion Diagrams to represent sequential arithmetic data-paths with registers. This extension allows TED to be used for register and delay minimization, while at the same time performing factorizations and common subexpression eliminations in the data-flow graph. It also enables transformation of one type of design into another, which is particularly useful in DSP design and filter optimizations. TED is shown as a valid framework for retiming and throughput optimizations. Finally, we show that TED can also be used to evaluate accuracy (and compute round-off error bounds) in fixed-point hardware architecture and to optimize the architecture in the presence of such errors under accuracy constrains. The proposed framework may be used to: (1) automatically compute the accuracy of a given architecture and certify (through a formal proof) that a given architecture meets or exceeds the required accuracy; and (2) optimize the architecture (in terms of delay, area, or power consumption) subject to the required accuracy. TED framework can provide a fast architectural exploration for DSP designs implemented in fixed-point hardware. In summary, this thesis will show that TED can be used as a kernel tool in high level synthesis that targets different optimizations and design transformations of data-flow designs. It can also be used as a vehicle to perform verification between the different forms of designs.

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