Title

Clock Generation and Distribution for Enhancing Immunity to Power Supply Noise

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Abstract

Clock generation and distribution are getting difficult due to increased die size and increased number of cores in a microprocessor. Clock frequencies of microprocessors have been increased and expected to trend 4GHz in near future. This increased clock frequency requires to limit the clock skew and jitter to 5~10% of clock frequency, which is 12.5~25ps. On top of this, non-ideal power supply behavior (supply droops) is worsening available timing margin to the critical paths. This dissertation presents three types of interrelated works: 1) analytical modeling of period jitter of global clock distribution induced by power supply droop, 2) circuit design of a power supply droop detector with 20mV resolution and 1 cycle latency, and 3) architectural studies regarding new adaptive clocking architectures which reduce the worst case period jitter and the worst timing slack. In the analytical modeling of period jitter in global binary clock tree, period jitter caused by power supply droop is formulated into recursive expressions based on propagation delay variation expressions. These recursive expressions are simplified into non-recursive expressions to pinpoint the location of the worst case period jitter in time domain. During this process, the physical relationship between the power supply noise and period jitter is studied extensively in time domain. The resulted analytical expressions can predict the period jitter in the clock distribution with only 5 ps error compared to HSPICE simulations. [1] [2] [3]. The study of period jitter in global clock distribution showed that the input period jitter into the clock distribution can be adjusted to improve the period jitter at the end of the clock distribution. To achieve input jitter modulation, a very fast supply droop detector is vital. To address this challenge, a droop detector system is designed based on a detailed study on high end microprocessor power supply network. The study shows that the detector system can detect the supply noise with 20mV resolution in only one clock cycle latency. [4]. My two works are combined to study new adaptive clocking architectures. Two types of adaptive clocking architectures are studied and the results show both architectures can improve the worst case slack by 10ps. This can be considered a significant improvement when it is compared to the traditional worst case based clocking.

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