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博士论坛

TTA结构数字信号协处理器数据Cache的设计与实现

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摘要 本文分析了面向多媒体应用的TTA（Transport Triggered Architecture）微处理器的特点和访存要求，提出并设计实现了应用于此款微处理器、采用直接映象规则、写回和按写分配策略的4KB数据Cache，并在全系统环境下对其进行了模拟验证。实验结果说明数据Cache系统在降低命中时间和提高命中率两方面做到了良好的折中，命中时间与芯片流水线处理周期匹配，有效保证了全系统性能的发挥。

关键词 TTA、数据Cache、直接映象、写回、按写分配

分类号

The Design and Implement of Data Cache for Digital Signal Coprocessor Based on TTA

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Abstract

The characteristics of Transport Triggered Architecture (TTA) were analyzed. The excellent process ability of TTA pipeline gave high demands to the data cache. A 4KB data cache system which used direct mapped principle, write back and write allocate strategies was proposed and implemented. The data cache combined with the TTA pipeline and other function units composed the whole TTA microprocessor. The microprocessor was simulated completely with real applications. The implementation results proved that the data cache in TTA microprocessor can achieve excellent trade-off for hit time and hit probability. The hit time can match the pipeline cycle and the high performance of the microprocessor was ensured.

Key words TTA Data Cache direct mapped write back write allocate

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