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Dynamic Resource Management For High-Performance Many-Core Packet Processing Systems

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Abstract
The complexity of operations performed in the data path of today's Internet has expanded significantly beyond the simple store-and-forward concept proposed in the original architecture. The trend towards more functionality and complexity in the data path is expected for next-generation networks in order to accommodate innovative applications that may emerge in the future. Flexible deployment of network

applications and sufficient processing capacity are therefore key to the success of next- generation packet processing systems. To develop such systems, three key questions need to be answered: (1) How to build them? (2) How to use them? and (3) How to utilize them. In this dissertation, I discuss my work in areas of network processor architecture design, programming abstraction, and runtime management.

Task graph is proposed as a simple programming model to separate network processing functionalities from resource management in order to exploit inherent parallelism presented in network processing. The abstraction of task is supported in hardware design to simplify software development. A novel network processor architecture is introduced in this dissertation to address key challenges of general programmability and high performance in next-generation data path. Further design extensions provide fair multithreading on individual cores for fine-grained hardware resource management.

With task graph, traditional monolithic processing workload of typical network protocols in data path is partitioned and analyzed. Based on this analysis, an efficient runtime management system is then designed to solve load-balancing problem on current many-core packet processing systems. As the number of integrated cores on many-core architecture keeps increasing in a steady pace, a distributed workload offloading mechanism is further designed for processing task mapping on large scale many-core systems.

Evaluation results show solid improvement in simplifying programming model, data path hardware resource utilization, and many-core scalability. With current industry shift towards many-core architecture and increasingly diversified network applications, this work represents an important step towards next-generation programmable packet processing systems.

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