西安电子科技大学学报 2006 33 (6): 990-994 ISSN: 1001-2400 CN: 61-1076/TN

基于非冗余排序的地址总线的功耗优化编码

孙海JUN, 邵志标

西安交通大学 电子与信息工程学院，陕西 西安 710049

收稿日期 修回日期 网络版发布日期 2006-12-12 接受日期

摘要 提出了一种新的低功耗非冗余排序总线编码方法，通过对改进的偏移地址线的动态重排以降低具有高负载的地址总线的功耗. 该编码方法根据偏移地址的值域对地址总线的低位进行优化重排，通过高位地址总线传送排序矢量至存储器的地址接收端，相对于传统的地址总线编码方法，具有更低的总线跳变率. 实验结果表明，采用所提出的非冗余排序总线编码，地址总线的跳变率降低了88. 2%，功耗减少了76. 1%，有效降低了地址总线的功耗.

关键词 低功耗 偏移地址 地址总线 总线编码 跳变

分类号 TP302

Power-optimal encoding of the address bus based on irredundant sorting

SUN Hai-jun,SHAO Zhi-biao

School of Electronics and Information Engineering, Xi’an Jiaotong Univ., Xi’an 710049， China

Abstract

<FONT face=Verdana>This paper presents a novel low-power address bus encoding method to reduce the transition activity on address buses and hence reduce power dissipation. The irredundant sorting bus encoding method reduces the power dissipation of highly capacitive memory address bus based on the dynamic reordering of the modified offset address bus lines. This method reorders the ten least significant bits of offset address according to the value of offset address, and the optimal sorting pattern is transmitted through the high bits of bus without the need for redundant bus lines. As compared to the conventional encoding methods, the proposed encoding method is superior in terms of transition activity reduction on the address bus. Experimental results by using an instruction set simulator and SPEC2000 benchmarks show that the irredundant sorting bus encoding method can reduce signal transitions on the address bus by 88. 2%, and that the power dissipation of the address bus is reduced by 76. 1%, which indicates that the proposed encoding method is very practical for power optimization of the address bus.
</FONT>

Key words low-power offset address address bus bus encoding transition activity

DOI:

通讯作者