研发、测试

高速误差扩散调频挂网芯片的设计与实现

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摘要　　在半色调处理的数字调频挂网处理方法中，误差扩散是一种效果非常好的算法，但是需要大量计算与存储器操作，处理速度是它广泛应用的主要瓶颈。通过设计专用芯片并且改进算法的执行步骤来加快基于误差扩散算法的调频挂网的处理速度。在设计中利用查找表（LUT），分级存储体系，流水线体系结构等技术提高挂网速度，从而每个时钟周期能够生成一个调频网点。结果表明，采用这种芯片可以有效地解决基于误差扩散算法的调频挂网方法的速度瓶颈问题。

关键词　　误差扩散　调频挂网　高速　查找表　流水线

分类号

Design and implementation of high speed error diffusion FM screening chip

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Abstract

　Among many methods to digital FM halftone process，the error diffusion algorithm is a very good one，but unfortunately it is computationally costly and uses much memory access．The processing speed is the main bottlenecks of its extensive use．This paper approaches a high speed error diffusion chip to accelerate the speed of the process．The design uses some techniques such as LUT（Look Up Table），hierarchical storage system and the pipelined architecture to speed up the process，finally it can process average one pixel per clock cycle．At last the chip is implemented in FPGA and shows that it solves the speed bottleneck of the error diffusion FM screening in high speed equipment．

Key words　 error diffusion　FM screening　high speed　LUT　pipeline

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