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研发、设计、测试

3D图形流水线像素处理后期的设计和实现

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摘要 针对3D图形流水线像素处理后期的实时大批量数据处理和存储器读写要求，以及嵌入式系统资源和功耗的特殊性，给出一种像素处理后期的硬件设计方案。设计首先实现所有测试功能，确保各种效果，其次采用了基于屏幕分割渲染的设计思想，减少存储器需求，然后吸收了Early Z算法，尽早抛弃不可见的三角面信息，减少渲染的数据，最后实现了Flip Quad反走样算法，提高图像的质量。模块已经完成了RTL级建模，并在FPGA上通过验证。

关键词 图形流水线 嵌入式图形 像素处理

分类号

Design and implementation of pixel processing back-end for 3D graphics pipeline

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Abstract

Considering the large quantities of data processing and memory access in pixel processing back-end of 3D graphics pipeline，as well as the strict resources and power consumption of embedded system，the paper presents a design of pixel processing back-end hardware.First，the design implements all the test function to ensure various effects；and second it adopts the idea of screen-split rendering，thus reduces the memory requirement；and thirdly it absorbs Early Z algorithm，which can help to abandon sightless triangular surfaces as soon as possible and reduce data amount；finally it realizes the Flip Quad anti-aliasing algorithm and improves image quality.All the RTL modules have been completed and verified on FPGA board.

Key words graphics pipeline embedded graphics pixel processing

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