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论文

阵列乘法器通路时延故障的内建自测试

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摘要
阵列乘法器因高度集成和高速运行，容易受到时延故障的困扰。该文对阵列乘法器的通路时延故障提出了一种用累加器实现的以单跳变序列作为测试序列的内建自测试方案。已有的理论和实践表明采用单跳变测试序列比多跳变序列具有更高的测试鲁棒性。同时，该文的测试方案在测试通路覆盖率和测试向量数之间做到了兼顾。仿真结果表明这种单跳变测试序列具有高测试通路覆盖率。此外，测试生成通过系统已有累加器的复用可节省硬件成本开销。

关键词 阵列乘法器 内建自测试 时延故障测试 通路时延故障 单跳变序列

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Built-in Self-Test Scheme for Path Delay Fault of Array Multiplier

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Abstract
Due to high integration and high speed operation, array multiplier much likely suffers from delay fault. In this paper, a Built-In Self-Test (BIST) scheme is presented for the delay fault test of such array multiplier in which an accumulator is utilized as test pattern generator. Based on the transition propagation analysis of the basic unit of full adder, a kind of single input change BIST sequences is generated which has been designated to be more effective than multiple input change sequences when highly robust delay fault coverage is targeted in a series of previous theoretical and experimental results. The proposed scheme is well balanced between the path coverage and the number of test patterns. Simulation results demonstrate the proposed scheme can get high path coverage. Furthermore, the reuse of existing accumulator to generate test patterns can lead to low hardware overhead.

Key words Array multiplier Built-In Self-Test (BIST) Delay fault test Path delay fault Single input change sequences

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