基于Verilog HDL语言的新型抢答器设计

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摘　要：本文提出一种基于Verilog HDL语言的抢答器设计方法。该设计实现有三组输入，具有抢答倒计时功能，对各抢答小组成绩进行加减操作并显示的抢答器。文中介绍抢答器设计架构、硬件电路和控制程序的设计方法。该抢答器采用Verilog HDL语言模块化和层次化的思想，使设计十分简单，能够广泛应用于各种竞赛中。

关键词：抢答器,Verilog HDL,层次化和模块化,FPGA,验证

The new design of answering device based on Verilog HDL

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Abstract: This article proposes a method to design a answering device based on Verilog HDL. The design achieves a answering device with three groups input and control of counting down. The answering device can also display the groups' grade and control it by addition or subtraction.The paper introduces the framework, hardware circuit and control program. The answering device applies the idea of the hiberarchy and module of Verilog HDL. So the design is very simple and can be applied to many competitions.

Key words: Answering device,Verilog HDL,Hiberarchy and module,FPGA,Validation