一种双线异或组成单元及其在VLSI电路设计中的应用

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提　要　本文介绍一种双线异或电路的构成单元，它能方便地向横向与纵向扩展，从而有利于VLSI电路的设计. 文中给出了采用该单元构成的具有自校验特性的3个电路的设计，它们是XOR阵列，比较器和择多表决器.

关键词　双线异或电路；VLSI电路；Tally电路；比较器；择多表决器；自校验
中图法分类号　TN47；TP302.8

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A Basic Building Cell of Dual-Rail XOR Circuit and Its Application in VLSI Circuit Design

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Abstract A basic building cell of dual-rail XOR circuit is presented, which is easy to bud horizantally and vertically, and will facilitate the VLSI circuit design. Several circuits constructed by these cells are shown, namely they are dual-rail XOR array, comparator and majority voting circuits. They all are of self-checking property.

Keywords dual-rail XOR circuit; VLSI circuit; daily circuit; comparator; majority voter; self-checking

1 Introduction

All decoding procedures for error detection or correction codes usually involve modulo 2 addition, i.e., the XOR operation. Commonly used XOR circuits in VLSI design are shown in [1]. The calculation of parity equation is then accomplished by an XOR tree or an XOR chain. Here, we present three new dual-rail circuits used in VLSI decoder designs. They are the XOR chain circuit, the comparator and the majority voter. All the circuits are constructed by nMOS FET. Because of the dual-rail property[2], they are self-checking circuits which will detect any single fault in the circuits. This occurs whenever the output pair has a violation to the patterns (1,0) or (0,1). Basically they use the pass transistor structure[3]. Thus the working speed for these circuits is higher than conventional circuits. Moreover the VLSI layout is very regular and easy to bud horizontally or vertically, especially when the circuits are used for matrix multiplication or syndrome calculation. Also, a smaller chip area is required.

2 Basic building cell

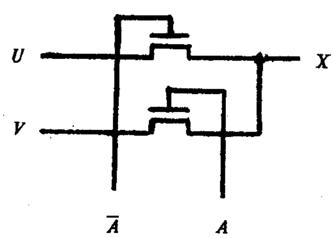

Fig. 1 Basic Building Cell

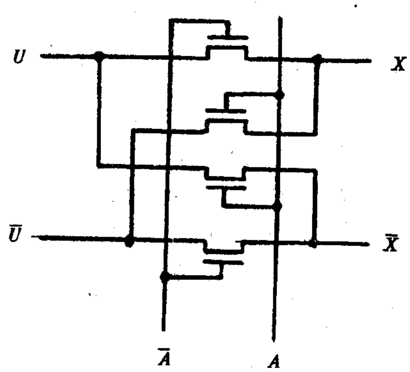

Fig. 2 Dual-rail XOR stage

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Refer to Fig. 1 , the output of this circuit, X, can be written as

$$X = U\overline{A} + VA.$$

This basic cell is used to construct an XOR ahain, a majority voting circuit and a comparator.

3 A dual-rail XOR chain

Let $V = \overline{U}$ in Fig. 1 and connect two such cells to form a single stage of an XOR circuit as shown in Fig. 2. This circuit functions as a dual-rail XOR circuit. Now we can cascade these stages to form an XOR chain as shown in Fig. 3

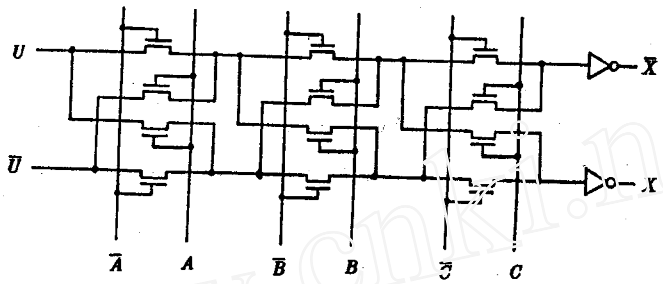

Fig. 3 Dual-rail XOR chain

$X = U \oplus A \oplus B \oplus C$ usually set U = 0

Because of the structure of pass transistors, a pair of invertors is inserted after every four stages of the actual XOR chain[3]. Fig. 4 shows the layout of a single XOR stage.

Fig. 5 shows the output response of a four-stage XOR chain obtained by SPICE computer simulation with the following nMOS parameters. Here, $\lambda = 2\ \mu m$, i.e., the minimum width $= 2\lambda = 4\ \mu m$.

```
.MODEL ENH1 NMOS LEVEL=2 LD=0.208U TOX=652E-10 NSUB=1.30E+15
+VTO=0.805 KP=2.95-05 GAMMA=0.415 PHI=0.6 UO=400 UEXP=1.0E-0.3
+UCRIT=5.92E5 DELTA=2.0 VMAX=1.0E5 XJ=0.88OU NFS=1.05E+12
+NEFF=1.0E-02 NSS=0 TPG=1 RSH=25.4 CGSO=1.6E-10 CGDO=1.6E-10
+CGBO=1.7E-10 CJ=1.1E-4 MJ=0.5 CJSW=1E-9
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.MODEL DEP1 NMOS LEVEL=2 LD=0.14OU TOX=652E-10 NSUB=1.189E+14
+VTO=-3.51 KP=2.83E-05 GAMMA=0.351 PHI=6.6 UO=916 UEX=1.0E-03
+UCRIT=8.05E5 DELTA=3.61 +VMAX=5.77E5 XJ=0.201U NFS=4.31E+12
+NEFF=1.0E-02 NSS=1.0+11 TPG=1 RSH=25.4 CGSO=1.6E-10
+CGDO=1.6E-10 CGBO=1.7E-10 CJ=1.1E-4 MJ=0.5 CJSW=1E-9
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4 A dual-rail majority voter

The majority voter is formed from a tally circuit[3]. The nMOS diagram of a tally circuit is shown in Fig. 6 , which implements a tally function with 3 inputs and 4 outputs. The kth output

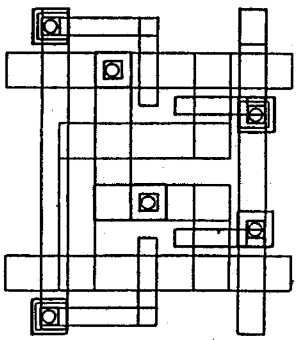

Fig. 4 Layout of Fig. 2

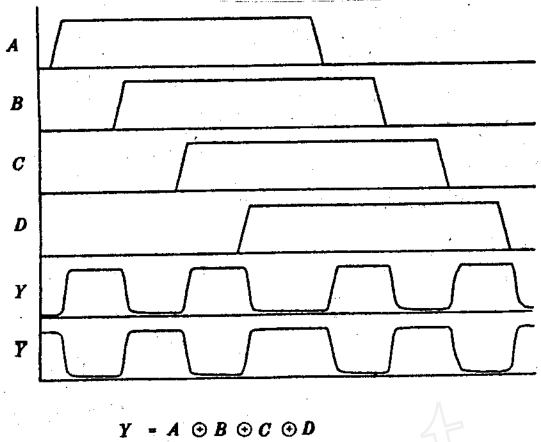

Fig. 5 Response of 4-stage dual-rail XOR chain

is to be high and all other outputs low if k of the inputs are high. The Boolean equations representing this function are

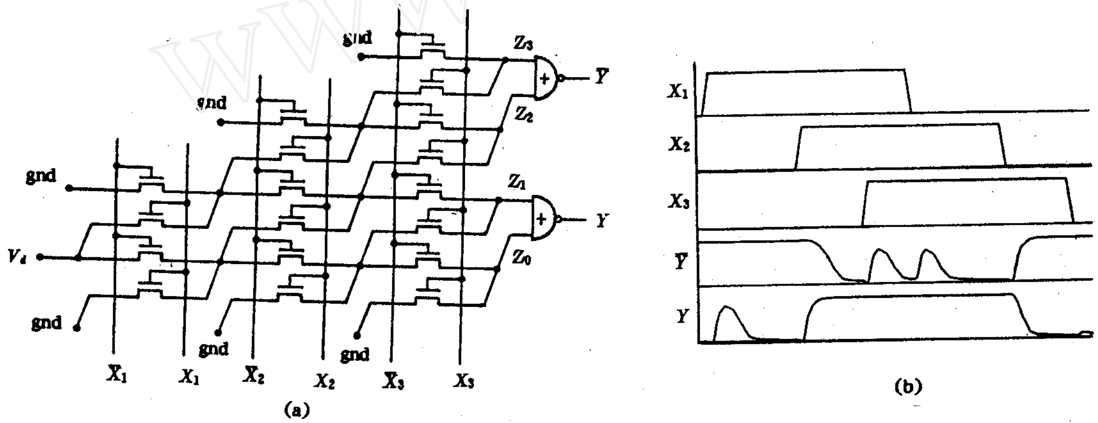

Fig. 6 Tally circuit and its response

$$\begin{cases} Z_0 = \overline{X}_1\overline{X}_2\overline{X}_3 \\ Z_1 = X_1\overline{X}_2\overline{X}_3 + \overline{X}_1X_2\overline{X}_3 + \overline{X}_1\overline{X}_2X_3 \\ Z_2 = X_1X_2\overline{X}_3 + X_1\overline{X}_2X_3 + \overline{X}_1X_2X_3 \\ Z_3 = X_1X_2X_3 \end{cases}$$

The outputs of a dual-rail majority voter then are formed by

$$\begin{cases} Y = Z_2 + Z_3 \\ \overline{Y} = Z_0 + Z_1 \end{cases}$$

Unfortunately, the original circuit shown in Fig. 6 (a) did not work properly. Fig. 6 (b) shows the output response by computer simulation in SPICE, with inputs having rise and fall times equal to 1 μs. It seems that the transient behavior of Z_i is much better in discharging than in recharging. This strikes us to switch the roles of V_d and gnd in order to improve the transient behavior, thus the negative logic of Z_i is used. The modified circuit is shown in Fig. 7 and the resultant output response is shown in Fig. 8. Here the inputs and the outputs still use positive logic. Fig. 9 is the layout of the dual-rail majority voter.

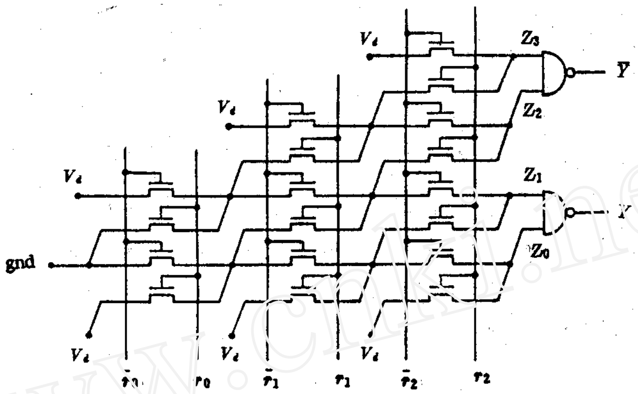

Fig. 7 Modified tally circuit

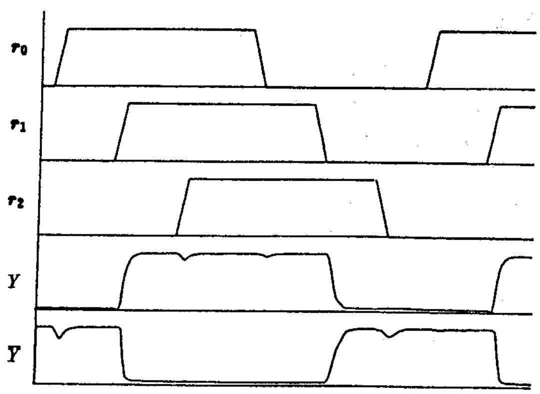

Fig. 8 Response of modified tally cirsuit

5 A dual-rail comparator

The comparator has n inputs and n outputs. It compares the input, an n-tuple vector $\underline{r}$, with the specified vectors $\underline{R_i}$, $i=0,\cdots,n-1$. If the Hamming distance between r and $\underline{R_i}$ is less than $d_c = k$, a specified value, then the kth output component y_k is set to 1; otherwise $y_k = 0$

The comparator works similarly to the tally circuit. Fig. 10 shows the citcuit configuration for output y_i which compares the input r with $\underline{R_i} = [0\ 1\ 1\ 1\ 0\ 0]$ for $d_c = 3$.

6 Self-checking property

For a fault model, we assume that the faults possibly occuring in the circuits are common

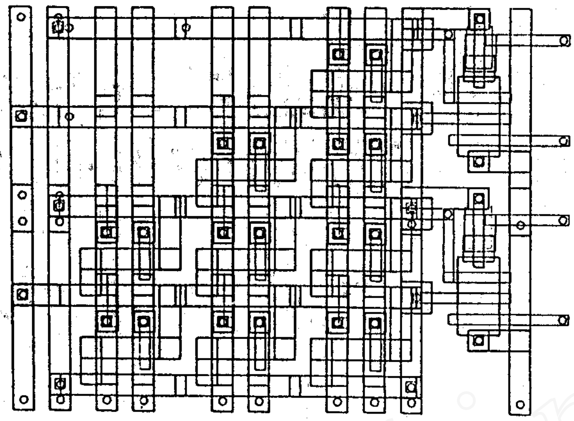

Fig. 9 Layout of dual-rail majority voter

ones, i,e. stuck-at-open-circuit and stuck-at-short-circuit. This is because MOS technologies do not simply exhibit the traditional stuck at 1 and stuck at 0 failure model[4]. It is assumed that at most one fault may occur in a circuit. Thus, the dual-rail structure guarantees that circuits will either give the correct output or flag a single fault[2].

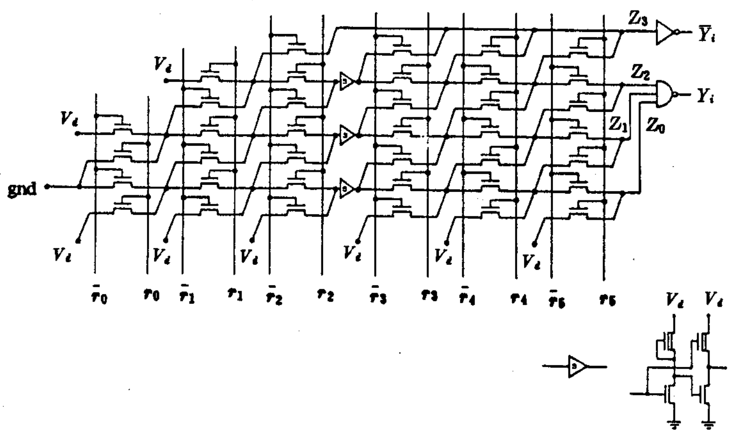

Fig. 10 Comparator

Referanoe

[1] S. Muroga, VLSI System Design, When and How to Design Very-Large-Scale Integrated Circuits, John Willy & Sons, 1982

[2] R. G. Bennetts and et al. , The Theory of Reliable System Design, 1983: 107

[3] C. Mead and L. Conway, Introduction to VLSI Systems, Addison-Wesley Publishing Company, 1980

[4] N. Micolaidis and et al. , Stronly Code Disjont Checkers, IEEE International Symposium on Fault-Tolerant Computing, FTCS-14, 1984