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组合型多电平变换器拓扑的研究

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Research on Combined Multilevel Converter Topologies

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ABSTRACT: To decrease the number of clamping devices in multilevel converters, a topology construction principle was proposed. Based on this principle, two novel types of multilevel converter topologies for medium voltage applications were researched. One was the combined multilevel converter topologies which were constructed by combining the conventional diode clamped or flying capacitor multilevel converters with two-level bridge legs; the other was a novel combination method for flying capacitor converters, which considered a tradeoff between the switching device number and capacitor voltage balancing. Both of the two types of multilevel converter topologies can produce more voltage levels with fewer switching devices. The reliability is improved and costs are saved. But some of the devices will block more than one DC-Bus capacitor voltages. So they are suitable for medium-voltage and high-performance requirement applications. The validity of the novel topologies is proven by simulated and experimental results.

KEY WORDS: power electronics; multilevel converter; topology; combined

摘要: 提出了以减少多电平变换器中箝位器件的数量为目的的拓扑生成原则，并基于该原则，研究了适用于中压场合的 2 类新型多电平拓扑。其中一类是通过组合传统的二极管箝位型或飞跨电容型拓扑与两电平桥臂得到的组合型拓扑；另一类是飞跨电容型拓扑的新型组合策略，它考虑了开关管数量和电容电压平衡之间的折衷。这 2 类新型拓扑都能以较少的器件输出较多的电平数，因此提高了系统可靠性，降低了成本。但是这 2 类拓扑的缺点是，某些器件需要承受大于 1 倍的单个电平电压，所以它们更适合于中压高性能的应用场合。仿真和实验结果验证了新型拓扑的有效性。

关键词： 电力电子；多电平变换器；拓扑；组合型

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0 INTRODUCTION

Multilevel converters can synthesize multi-staircase output voltage by combining several DC-Bus capacitor voltages，so they have better harmonic spectra and lower device voltage stresses. They are particularly suitable for high-voltage and high-power applications. However，the conventional multilevel converters will require more clamping diodes or flying capacitors to increase the number of voltage levels，so the number of the achievable voltage levels is limited due to circuit layout and packaging constraint.

In recent years，there is a new direction to construct novel multilevel converter topologies，which can produce higher quality waveforms with fewer devices[1-13]. In this paper，the construction principles of these topologies are summarized and two types of novel topologies are researched.

1 CONSTRUCTION PRINCIPLES OF THE NOVEL MULTILEVEL CONVERTER TOPOLOGIES

For an *n*-level converter topology，the number of devices used is expected to be minimum. Generally speaking，in diode clamped and flying capacitor multilevel converters，the devices used include power switches，clamping diodes，flying capacitors and DC-Bus capacitors. The maximum number of output voltage levels is decided by the number of DC-Bus capacitors. So *n*–1 DC-Bus capacitors are required for an *n*-level output voltage topology. After determining the number

of DC-Bus capacitors，we can only change the topology structure to reduce the number of power switches and clamping devices. In diode clamped and flying capacitor multilevel converters，the number of power switches does not increase largely with the increase of voltage level numbers，while the number of clamped diodes and flying capacitors increases largely. Therefore，the main aim is to reduce the clamping devices.

The highest and lowest voltage levels are obtained by connecting the positive bus and negative bus to the output terminal through a certain group of power switches respectively. However，there are many kinds of connections for the middle voltage levels，which will be an important clew for structure change. In the conventional diode clamped and flying capacitor multilevel converters，all the middle voltage levels are realized through clamping devices. If some of the voltage levels are realized through fewer clamping devices，even no clamping devices，then the number of clamping devices will be reduced largely. Based on this principle，two types of multilevel converter topologies are obtained in this paper and their structure characteristics and operation principles are researched in detail.

2 COMBINED DIODE CLAMPED AND COMBINED FLYING CAPACITOR MULTI-LEVEL CONVERTER TOPOLOGIES

Fig.1 is the combined diode clamped multilevel converter topology，which is obtained by replacing the positive bus，negative bus and neutral points with two-level bridge legs. Fig.2 shows a combined flying capacitor five-level converter. It is composed of a conventional three-level flying capacitor converter bridge leg and two two-level bridge legs. Some of the middle voltage levels of the two combined topologies can be produced only by main power switches，so fewer clamping diodes and flying capacitors are required than the conventional multilevel converters at the same number of output voltage levels. Their detailed construction rule，modulation methods，advantages and disadvantages have been discussed in Ref.[1]. A combined flying capacitor five-level half-bridge inverter prototype is constructed in the laboratory. The switching frequency of the main bridge leg switches is 1.5kHz, and the switching frequency of the clamping bridge leg switches is 3kHz. The modulation index is set to 0.8. Fig.3 shows the

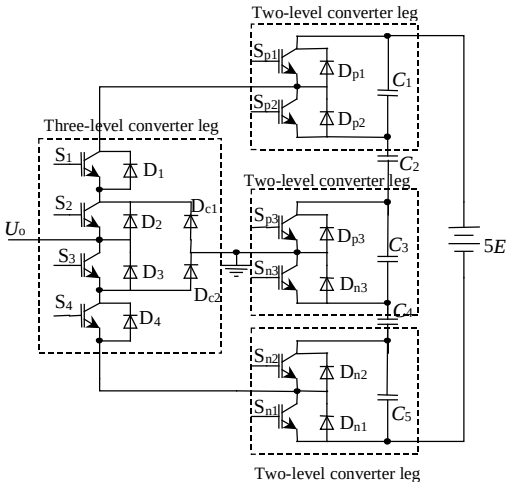


图 1 二极管箝位组合型七电平变换器

Fig.1 Combined diode clamped seven-level converter

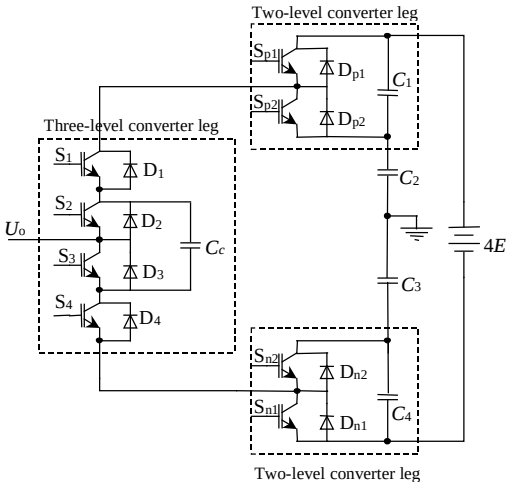
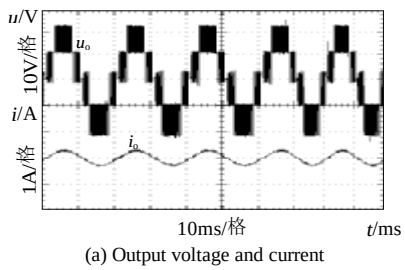
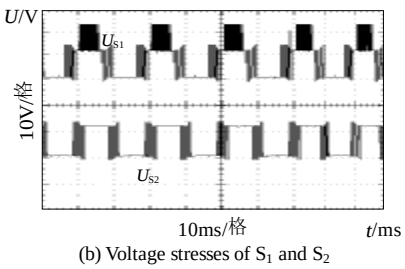


图 2 飞跨电容组合型五电平变换器

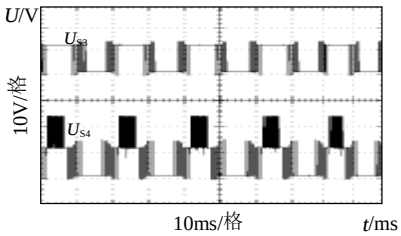
Fig.2 Combined flying capacitor five-level converter



(a) Output voltage and current



(b) Voltage stresses of S_1 and S_2



(c) Voltage stresses of S_3 and S_4

图 3　飞跨电容组合型五电平逆变器的实验波形

Fig.3　Experimental waveforms of the combined flying capacitor five-level inverter

experimental results of output voltage, output current and voltage stresses of the main bridge leg switches.

3　A NOVEL COMBINATION SCHEME FOR FLYING CAPACITOR MULTILEVEL INVERTERS

In the conventional flying capacitor multilevel converters，the voltage difference between two nearer flying capacitors is equal to one voltage level. So the nearer flying capacitor voltages are arranged by one voltage level and all the capacitors have the same capacitance and voltage ratings[14-15]. In these topologies，there are redundant switching states for middle voltage levels. The voltage synthesis flexibility provides possibility for capacitor voltage balancing[16]. However，this case will result in fewer output voltage levels with large numbers of switching states. In fact，the output voltage can be synthesized by combining different capacitor voltages，so the voltage difference between two nearer capacitors need not always be one voltage level.

To utilize all the switching states，a full binary combination schema for floating voltage source multilevel inverters was proposed in Ref.[4]. Its main idea is to make one switching state corresponding to one output voltage level by changing the capacitor voltage ratios. Thus more output voltage levels can be realized by using fewer switching devices. But the disadvantage of this schema is that the capacitor voltage balancing is difficult to realize，so separated voltage sources are used to replace the flying capacitors. Therefore it is more suitable for power supply systems with batteries. Although the capacitor voltage balancing of a three phase topology can be realized through complex control，the modulation index will be limited[5].

By considering a tradeoff between the switching device number and capacitor voltage balancing，a novel capacitor voltage combination method is proposed in this paper. The voltage ratio and number of output voltage levels of the novel combination method are between the ones of conventional topology and full binary combination topology. In the proposed combination method，there are also redundant switching states for one certain middle voltage level. Thus more voltage levels can be produced and at the same time，some of the capacitor voltage can be balanced by using the redundant switching states.

The voltage ratio of the flying capacitors can be set according to equation (1)，where n_c is the number of two-switch cells，n_m is the maximum value in the voltage ratio. Then n_m+1 output voltage levels can be achieved.

$$u_i = j/n_m \cdot E,\ 1 \le i \le n_c, 1 \le j \le n_m, u_i < u_{i+1}, u_{n_c} = E \quad (1)$$

For example，for a three-cell topology，suppose the maximum value in the voltage ratio is five，that is to say，n_c=3，n_m=5，then the voltage ratio of the three cells u_1: u_2: u_3 may be 1:2:5, 1:3:5, 1:4:5, 2:3:5, 2:4:5, 3:4:5. Their corresponding switching states are shown in Tab.1.

表 1　三单元飞跨电容型拓扑输出六电平时的各种开关状态组合

Tab.1　Switching states of the three-cell flying capacitor converter with six-level output

output voltage	u_1: u_2: u_3																	
	1:2:5			1:3:5			1:4:5			2:3:5			2:4:5			3:4:5		
	S_1	S_2	S_3	S_1	S_2	S_3	S_1	S_2	S_3	S_1	S_2	S_3	S_1	S_2	S_3	S_1	S_2	S_3
E	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
$4E/5$	1 1	1 0	0 1	1	1	0	0 1	1 1	1 0	1	0	1	0	1	1	0 1	1 0	1 1
$3E/5$	1	0	0	0 1	1 0	1 1	0	1	0	0 1	1 1	1 0	1 1	1 0	0 1	0	0	1
$2E/5$	0	1	1	1 0	0 1	0 0	1	0	1	0 1	0 0	1 0	0 0	0 1	1 0	1	1	0
$E/5$	0 0	0 1	1 0	0	0	1	0 1	0 0	1 0	0	1	0	1	0	0	1 0	0 1	0 0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

It can be seen from Tab.1 that the same topology can produce six-level output voltage with different voltage ratios. And there are redundant switching states for some of the middle voltage levels. The different voltage ratios can be achieved when the topology produces other-level output voltage. The maximum output voltage level is 2^{n_c}, the case of full binary combination. To compare their differences, the switching states of the three-cell flying capacitor converter with five-level output are given in Tab.2.

表 2 三单元飞跨电容型拓扑输出五电平时的各种开关状态组合

Tab.2 Switching states of the three-cell flying capacitor converter with five-level output

output voltage	v_1: v_2: v_3								
	1:2:4			1:3:4			2:4:4		
	S_1	S_2	S_3	S_1	S_2	S_3	S_1	S_2	S_3
E	1	1	1	1	1	1	1	1	1
$3E/4$	1	0	1	0	1	1	0	1	1
	1	1	0	1	1	0	1	0	1
$2E/4$	0	1	1	1	0	1	0	0	1
	1	0	0	0	1	0	1	1	0
$E/4$	0	0	1	0	0	1	1	0	0
	0	1	0	1	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0

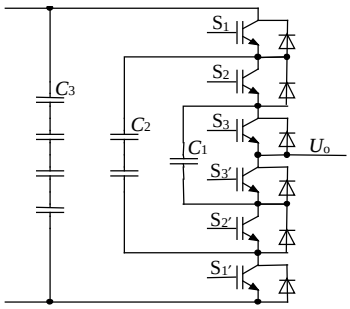
It is easier to balance the capacitor voltages if the number of redundant switching states is larger. For the novel combination method, there are redundant switching states for some of the middle voltage levels, so it is possible for the capacitor voltages to be balanced. In the following part, the case of u_1: u_2: u_3 = 1:2:4 will be used as an example to illustrate the capacitor voltage balancing.

To explain it clearly, Fig. 4 (a) shows a five-level one-leg inverter, in which all the capacitors have the same capacitance and voltage. Tab.3 illustrates the corresponding switching states and capacitor paths. It can be seen from the table that the voltage of C_1 is influenced by the voltage levels of E and $3E$, and the voltage of C_2 is influenced by the voltage levels of $2E$ and $3E$. For C_1, there exist a charging path and a discharging path for $3E$ and E respectively, so its voltage can be balanced if the charging and discharging time keeps equal. For C_2, except for a charging path and a discharging path for $2E$, another charging path is corresponding to $3E$ and the path for E. Because the charging time and discharging time for different voltage levels is difficult to keep same, its voltage is difficult to be balanced. Thus Fig.4 (a) can be changed to Fig.4(b), i.e., C_2 is replaced by a DC voltage source and C_1 keeps unchanged. The problem of some devices sustaining higher voltage stresses still exists in this combination method. In Fig.4, S_1 and $S_{1'}$ will sustain double voltage level stresses.

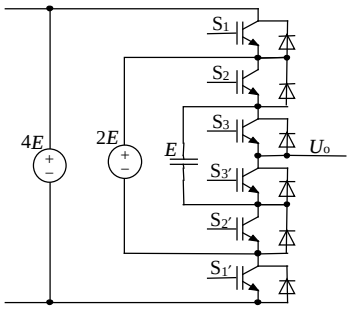
表 3 电容电压按照 1:2:4 组合的五电平拓扑开关状态和电容路径

Tab.3 Switching states and capacitor paths of the five-level inverter with u_1: u_2: u_3=1:2:4

output voltage	S_1	S_2	S_3	capacitor path
$4E$	1	1	1	C_3
$3E$	1	1	0	C_3–C_1
	1	0	1	C_3– C_2+C_1
$2E$	0	1	1	C_2
	1	0	0	C_3– C_2
E	0	0	1	C_1
	0	1	0	C_2– C_1
0	0	0	0	——



(a)Original topology

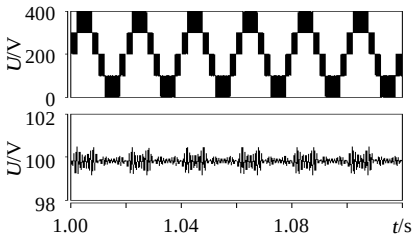


(b)Changed topology

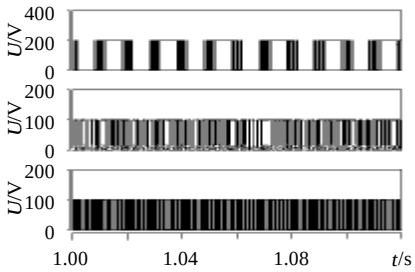
图 4 电容电压按照 1:2:4 组合的五电平单臂电路

Fig.4 Five-level topology with u_1: u_2: u_3=1:2:4

To verify the validity of the novel combination method, the topology shown in Fig.4 (a) is simulated [17-20]. Fig. 5 shows the simulated results. It can be seen from Fig.5(a) that five voltage levels are produced and the voltage of C_1 is well balanced. Fig.5(b) shows that S_1 blocks double voltage levels in



(a) Output voltage and the voltage of flying capacitor C_1



(b) Voltage stresses on S_1, S_2 and S_3

图 5　三单元五电平拓扑中新型组合策略下的仿真结果

Fig.5　Simulated results of the novel combination method

off state，and S_2，S_3 only block one voltage level.

Based on the above analysis，the following conclusions can be drawn:

（1）There are multi-voltage-ratio setting methods in the novel combination method. The number of output voltage levels lies on the maximum value of the ratio. With more voltage levels，there are more voltage ratio setting methods.

（2）In some cases，the voltages of some of the flying capacitors can be balanced. The condition that these cases must be satisfied is that the voltage difference between this flying capacitor and the nearer two flying capacitors should be one voltage level. That is to say，the following equations should be satisfied:

$$u_i - u_{i-1} = u_{i+1} - u_i = E,\ \ 1 < i \le n_c \qquad (2)$$

$$u_{i+1} - u_i = E,\quad i = 1 \qquad (3)$$

where E is one voltage leve1

（3）For a same topology structure，if fewer voltage levels are produced，then more flying capacitors can be voltage balanced; otherwise，if more voltage levels are produced，then fewer flying capacitors can be voltage balanced. This is also the tradeoff between the number of output voltage levels and capacitor voltage balancing.

（4）The voltage stress of the main switching devices is the voltage difference between the two near flying capacitors. If the voltage ratio of the two capacitors is larger，the voltage stress of the corresponding main switching device is higher.

4　CONCLUSION

Two types of novel multilevel converter topologies for medium voltage applications are discussed in this paper. Both of the two types of novel multilevel converter topologies can produce more voltage levels with fewer switching devices. The reliability is improved and the costs are saved. But some of the devices will block more than one DC-Bus capacitor voltages. So they are more suitable for medium-voltage and high-performance-requirement applications. The two novel types of topologies provide a new application direction for multilevel converters. The capacitor voltage balancing method for the novel topologies and their fault tolerant design should be considered in the following research.

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