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PWM 变换器跟踪控制的双重Δ调制新方法

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A Novel Method of Double Delta Modulation on Tracking Control of PWM Converters

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ABSTRACT: Nonlinear tracking control is one of the important control strategies for PWM converters. A novel method of "double *d* modulation" for tracking control is proposed first, in which an error hysteresis-less comparator and a switch period timer are only needed. The comparator produces the fore-edges of the output PWM signal, which make faster response and higher precision, and the timer decides the back-edges, which ensure constant switch frequency. A period-by-period predicting arithmetic for the variable threshold of the hysteresis-less comparator is also proposed so that the average tracking error in any switching period is always zero, and the sub-oscillation and step out are suppressed. Simulation researches of voltage tracking control in three-phase four-line voltage sag compensating system validate the new strategy, and finally the experimental results for current tracking in a single-phase half- bridge inverter demonstrate the good tracking control performances.

KEY WORDS: power electronics; double *d* modulation; tracking control; pulse width modulation; threshold prediction; voltage sag

摘要：非线性跟踪控制是 SPWM 变换器的重要控制策略之一。提出了一种新型双重Δ调制跟踪控制方法，它由一个无滞环比较器和一个载波周期定时器组成。比较器产生 PWM 信号的上升沿，使得跟踪控制响应快，精度高；定时器决定 PWM 信号的下降沿，它保证了开关周期固定不变；文中提出了一个按周期对比较阈值进行预估调节的算法，该算法可使每个周期的平均跟踪误差均为零，同时可以抑制子谐振和跟踪失步。对三相四线电压跌落补偿系统电压跟踪的仿真研究证实了"双重Δ调制"策略和比较阈值的一步预估算法的有效性。最后对一个单相半桥逆变器的电流跟踪控制给出了实验结果。

关键词：电力电子；双重Δ调制；跟踪控制；脉宽调制；阈值预估；电压跌落

0 INTRODUCTION

Tracking control, current tracking or voltage tracking, is one of the important control strategies for PWM converters, it have been broadly applied in the area of electronic power conversion. There are mainly two kinds of basic methods for tracking control[1]. The first kind of them, called as linear method, is based on the output error linear regulation and triangular carrier modulation, it has advantages of exactly constant switch frequency, but there are some disadvantages of slower in response and more complicated in circuit[1-3].

The second kind, called as non-linear method, directly produces PWM signals by comparison between the reference input and real output. The non-linear tracking method includes amplitude modulation by hysteresis comparator[4] or time modulation by error comparison plus period timing[5-7]. They have common advantages of simplicity in circuit, rapidness in response and good in tracking precision and robustness; but there is visible fluctuation in their switch frequencies.

Aiming at the problem of switch frequency fluctuation many researchers have done excellent contributions. Regulating the hysteresis band dynamically by a switching frequency feedback controller can make the switching frequency constant in steady state. Furthermore prediction and feed

forward controls of the hysteresis band can make the frequency more stable[8-9]. A so-called ramp control method proposed by Kadjoudj, M. et al can make frequency constant, but the tracking error was not satisfying[10]. A. V. Anunciada and M. M. Silva have proposed a better scheme, combining a constant hysteresis band comparator and a timing clock of constant frequency in 50% duty cycle together and only one of the upper or lower thresholds indefinitely being used, it can realize a constant frequency but may produce larger errors, especially in a higher frequency sinusoidal reference condition[11]. Furthermore, Malesani L, et al improved the aforementioned scheme, the hysteresis band being regulated in real time period-by-period, this can make the tracking precision higher but the arithmetic was somewhat complicated[12]. Recently other new type tracking control strategies are contin- uously proposed for multilevel PWM converters[13-15].

A novel method so called "double *d* modulation" has been proposed by the authors of this paper, which is composed of a hysteresis-less comparator and a switch period timer, so it can realize both the tracking amplitude error regulation (amplitude *d* modulation) and the switch period timing (time *d* modulation). The "amplitude modulation" ensures rapid response and higher tracking precision and the "time *d* modulation" can realize exactly constant frequency[16]. In this paper, the subject is further studied in detail. In section II the basic principle of "double *d* modulation" is introduced. Then a new one-step predictive arithmetic for the comparing threshold is presented in section III. Taking a three-phase four-line voltage sag compensation system as example[17], in section IV simulation results are shown in detail. Section V gives corresponding experimental results. Finally, section VI concludes this paper.

1　BASIC PRINCIPLE OF "DOUBLE Δ MODULATION"

Fig. 1 shows a sketch of "double modulation" for tracking control. It consists of the combination of a hysteresis-less comparator with a variable threshold (denoted as *h*) and a switch period (denoted as *T*)

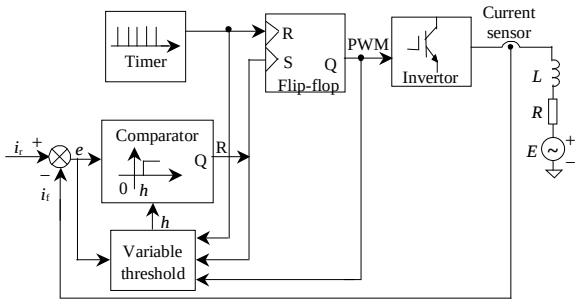


图 1　"双重*d* 调制" 原理示意图

Fig.1　A sketch of "double *d* modulation"

timer. The comparator, whose input is the difference between the input reference and the output feedback, achieves the "amplitude *d* modulation" and outputs a positive narrow pulse sequence, denoted by *R*. The timer implements the "time *d* modulation", and produces a positive narrow pulse sequence too, denoted as *F*. A R-S flip-flop synthesizes these two modulating action together and then exports the required two-level PWM signal of which *F* synchronizes the Falling edges and *R* decides the rising edges. An inverter controlled by the PWM signal exports the desired outputs. The tracking control object can be current or voltage, which is determined by the engineering requirement.

Fig. 2 shows a set of basic principle waveforms corresponding to Fig. 1, where the thin solid lines indicate input references i_r and the threshold *h*, the toothed thick lines indicate the tracking output feedback i_f or tracking error *e*, *T* is the switch period and T_1 is the time interval during which the PWM signal is in high level. The threshold *h* decides the rising edges of the two-level PWM, which are synchronized by *R* pulse sequence. The timer decides the falling edges of PWM, which are synchronized by *F* sequence. There is another alternative choice that the threshold decides the falling edges and the timer decides the rising edges. It is evident that the comparator ensures the faster response and higher control precision; especially the timer ensures an exactly constant switch frequency.

The double modulator uses the simplest hysteresis-less comparator; only one side threshold of the tracking error is controlled. So if the threshold *h* is constant the tracking error will have an average value,

which is not desirable, as shown in Fig. 2 (a). In order to cancel the average tracking error period-by-period, predicting and modifying of the threshold will be necessary. Fig. 2 (b) presents the effect of variable threshold, in which the threshold is adjusted period-by-period so that the average tracking error will always be zero.

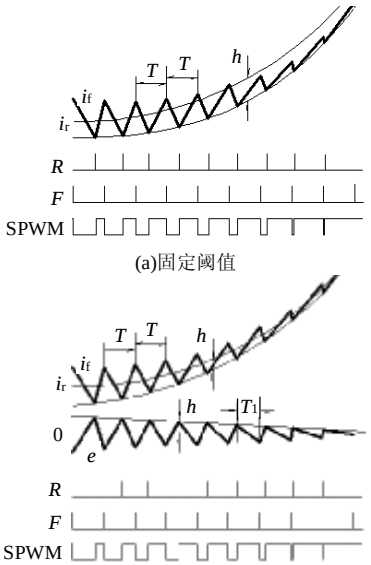


图 2 图 1 的原理波形

Fig.2 Basic principle waveforms of Fig.1

2 PREDICTING ARITHMETIC FOR THE VARIABLE THRESHOLD

The predicting arithmetic principle is shown in Fig. 3. In the figure, T, T_1, and e are the same meaning as in Fig. 2 (b); the thick line expresses the practical error that may has an average error within some particular switch period; h_1, h_2, and h_3 are respectively the instantaneous values of the error corresponding to the particular time points as defined in the figure; the thin line expresses the corresponding ideal error curve that has a zero average error in any period, of which $h_5=-h_4$ are the upper and lower practical thresholds, and T_2 is the desired high level interval; particularly h is the predicted threshold for the next switch period, using which the error will reaches the ideal condition at the end of the next period even though the error curve is not ideal in current period. So whether the practical tracking errors are, it will be in the ideal condition only after one switch period.

Generally we can consider that the error curve's

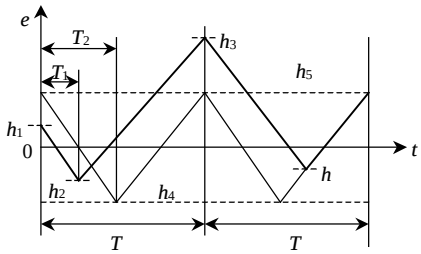


图 3 调节阈值的预估算法原理

Fig.3 The predicting arithmetic principle for variable threshold

rising and falling slopes are kept constant on any neighboring two switching periods. So from the current switch period, the first period in Fig. 3, the following equations can be derived

$$s_1=(h_2-h_1)/T_1 \tag{1}$$

$$s_2=(h_3-h_2)/(T-T_1) \tag{2}$$

$$h_5=-h_4=-\frac{s_1s_2T}{2(s_2-s_1)} \tag{3}$$

where s_1 and s_2 are the falling and rising slopes of the tracking error e respectively. From the second period in Fig. 3, the following equation comes into existence

$$(h-h_3)/s_1+(h_5-h)/s_2=T \tag{4}$$

From Equ.(4) the predicted threshold h can be obtained as Equ.(5), using which the practical error will reach the ideal point at the end of the next period

$$h=(s_1s_2T+s_2h_3-s_1h_5)/(s_2-s_1) \tag{5}$$

Fig. 4 gives a predictive calculation procedure. From Equ.(1) through Equ. (5) and Fig. 4, only two newer parameters, T_1 and h_3, need to be detected at every switch period, and have total five input parameters. Whole calculation requires six times of addition and eight times of multiplication. From Fig. 3, h_1 and h_2 are the h_3 and h in the last period respectively, and T, the timing period of carrier frequency, is a constant.

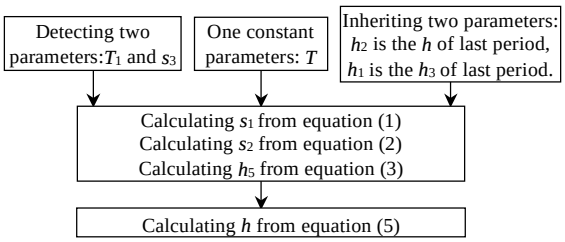


图 4 预估算法计算过程

Fig.4 Predicting calculation procedure

3 SYSTEM SIMULATION

3.1 Simulation system topology

This section shows the simulation research work

using PSCAD in an engineering application system of voltage sag compensation[17].

The simulation system topology is shown in Fig. 5. That is a three-phase four-line voltage sag compensating system. Only phase A is shown in detail, and the other two phases are symmetrical with phase A. A half bridge inverter is used in series connection with the incoming source line of phase A. Other two source lines of phase B and phase C are connected to the middle points of the two-diode legs respectively. Two line-to-line voltages charge the capacitors in the inverter. A bypass switch composed of two anti-paralleled thyristors is connected with the inverter in parallel. During the normal voltages, the bypass switches are closed, delivering utility power directly to the load. When voltage sags happen, the inverters operate, the bypass switches being open, and the output of the inverters supply the missing voltage and help in maintaining rated voltage at the terminals of the load[17].

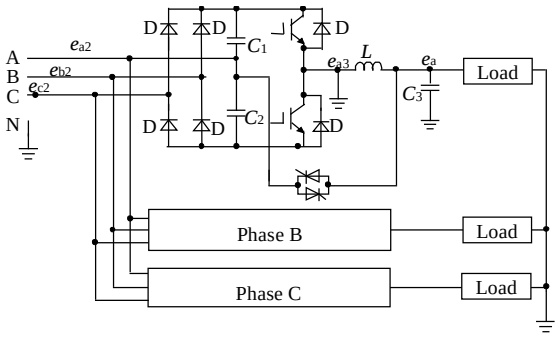


图 5　仿真系统的主电路拓扑

Fig.5　Main circuit topology of the simulation system

3.2　Control system and parameters design

The principle of the control system is almost the same as shown in Fig. 1, but some changes must be done as shown in Fig. 6. Firstly the tracking control objects are not currents, but the phase-to-neutral output voltages in loads, denoted as e_a, e_b and e_c as shown in Fig.5 or as u_o in Fig.6. Secondly the feedback variables are not directly the load voltages, but the voltages before filtering. If the load voltages in capacitor C are directly used as the feedback variable, the fast tracking control will be difficult as the resonant property the LC filters.

The system parameters in Fig.6 are as followings, power source frequency f_s=60Hz, power source line-to-line voltages U_s=200V/ms, carrier frequency (i.e. the frequency of the timer in the "double d modulation") of the SPWM inverter f_c=10kHz, rating capacity 3kVA of total three phases, DC capacitors in the inverters 470μF. Choosing L=10mH and C=3.3μF takes natural resonant frequency 876Hz and a unit damp factor.The first-degree low-pass filter has a time constant of 0.2ms.

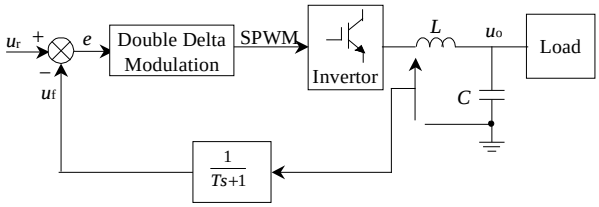
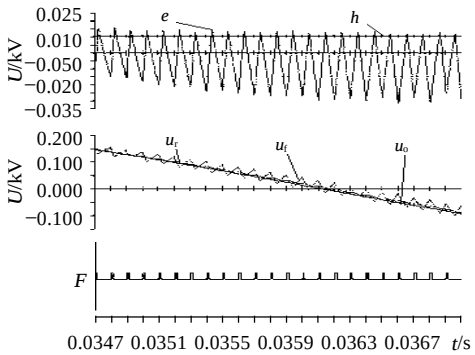


图 6　一相"双重d 调制"示意图

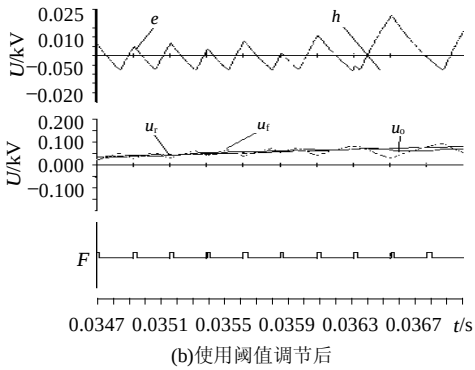
Fig.6　Control system scheme for one phase

3.3　Simulation results

Fig. 7 gives a simulation example, where the upper curves are the tracking error e and threshold h; middle curves are the reference input u_r, output feedback u_f and the practical output u_o after output filtering; and the lower curves are the switch period timing pulse sequences. Fig. 7 (a) is for the case of constant threshold. Fig. 7 (b) is for the case of after



(a)固定阈值时的跟踪误差



(b)使用阈值调节后

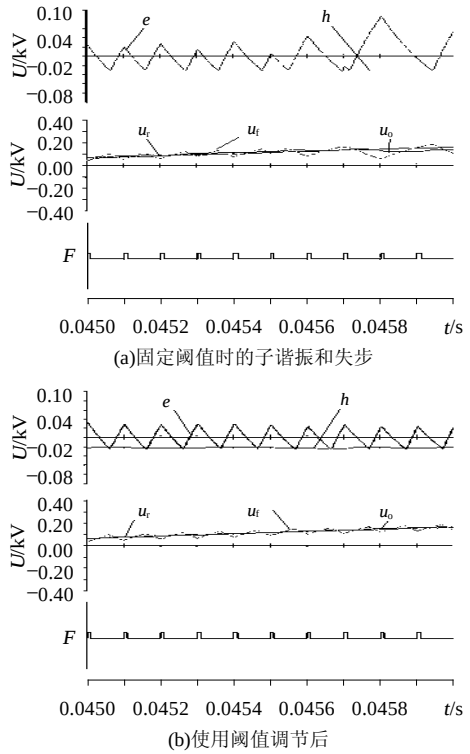
图 7　通过预估阈值来消除平均跟踪误差

Fig.7　Canceling the average tracking error by prediction of the threshold

predicting calculation as in Fig. 4 and modifying the threshold period-by-period in real time in the exactly same system parameters as Fig. 7 (a). It is evidently seen that Fig. 7 (a), with a constant threshold, has obvious average tracking errors but Fig. 7 (b), with a variable threshold, almost don't have any visible average errors. Furthermore the switch frequency are exactly constant which is synchronized by the timing sequence *F*.

Another simulation results are given in Fig. 8, the curves have the same meaning as for Fig. 7. Fig. 8 (a) is for the case of constant threshold too. In the figure, not only the positive and negative errors are not symmetrical, but also the PWM tracking control may have a sub-oscillation as shown in the middle time period, especially it may lose its steps as shown in the end period of Fig. 8 (a). Fig. 8 (b) is for the case of after predicting and modifying the threshold in the exactly same system parameters as Fig. 8 (a). It is evidently showed that the sub-oscillation and step out are suppressed well with a variable threshold.

Fig. 9 is a system simulation result, in which two phase-to-neutral voltages sag down to 17% and other



(a)固定阈值时的子谐振和失步

(b)使用阈值调节后

图 8 通过预估阈值来抑制子谐振和失步

Fig.8 Suppressing the sub-oscillation and step out by prediction of the threshold

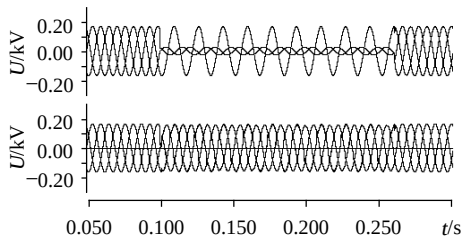


图 9 A 和 C 相电压跌落到 17% 但 B 相保持额定时的仿真结果

Fig.9 Simulation results with phase-A and phase-C sagged down to 17%, but phase-B normal

one phase maintaining normal. In the simulation, the loads are resistors of 13.5Ω. In the figure, the upper waveforms are the sagged incoming phase-to-neutral voltages; the lower waveforms are the load side phase-to-neutral voltages after compensation. From the figures we can see the properties of voltage tracking control.

Fig. 10 is for the various important variables in phase-A concerning with the "double *d* modulation" in the same simulation as that in Fig. 9. In this figure, e_{fa} is the feedback variable of phase A, corresponding to u_f in Fig. 6 and Fig. 8 or i_f in Fig. 1. e_{fa} comes from e_{a3} by the first-degree low pass filter as shown in Fig.6. e_{a3} is a sum of the SPWM output of the inverter and the residual phase-to-neutral voltage in phase A, so the SPWM levels of e_{a3} are not constant. e_{ra} is the reference input of voltage in phase A, corresponding to u_r in Fig 6 and Fig. 8 or i_r in Fig. 1. e_{ea} is the tracking error and h_a is the comparator's threshold. F_a and R_a are the narrow positive pulse sequences of the "double *d* modulator" in phase A, corresponding to *F* and *R* in Fig. 1, respectively.

From Fig.10, we can see the threshold is modified period-by-period, so that the tracking error is

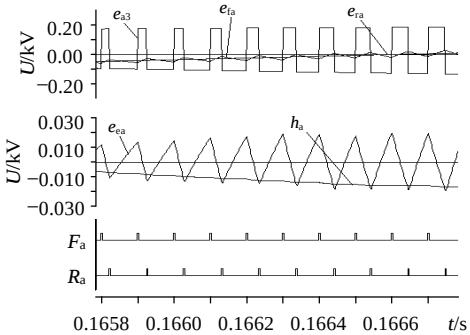


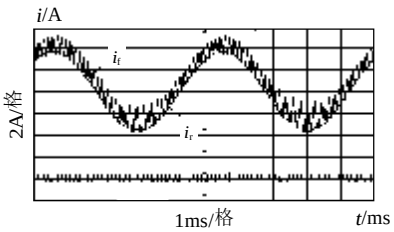
图 10 图 9 仿真中与"双重*d* 调制"相关的 A 相各主要变量

Fig.10 Variables in phase-A concerning with the "double *d* modulation" in the same condition as Fig.9

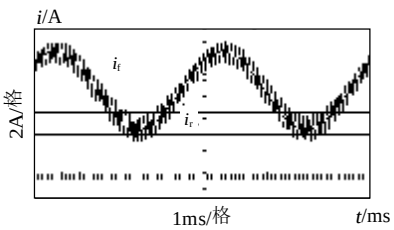
always symmetrical to zero in every switching period.

4 EXPERIMENTAL RESULTS

For a single-phase half-bridge inverter with *RL* load, Fig. 11 shows the experimental results of current tracking control, in which "double *d* modulation" as shown in Fig. 1 was used. The dc bus voltages were positive and negative 50V, R=6.6Ω, L=1.8mH, carrier frequency (the frequency of F pulse sequence as shown in fig. 1) was 10kHz. Fig. 11 (a) was for the case of constant threshold (was zero in this case), (b) was the case after using threshold predicting regulation. In the figures the upper curves were the reference current input i_r and output feedback current i_f, and the lower curve was the timing pulse sequence F used for time d modulation.



(a)固定阈值时的子谐振和失步



(b)使用阈值调节后

图 11　实验结果

Fig.11　Experimental results

It is evident from the figures that there were average tracking errors, sub-oscillation and tracking step out if using a constant threshold, and after the threshold predicting regulation the average error, sub-oscillation and step out were all suppressed.

5 CONCLUSION

This paper proposes and studies in detail a novel method of "double *d* modulation" for tracking control of PWM converters. The "double *d* modulation" is the combination of a simpler hysteresis-less comparator and a switching period timer. The former results in faster in response and higher in tracking precision, and the later ensure an exactly constant carrier frequency. An effective predicting arithmetic to the variable threshold is also proposed in this paper, which can suppress the average tracking error, sub-oscillation and step out.

Simulation studies in a three-phase four-line voltage sag compensating system had been done. The simulation results validate the proposed new control strategy as well as predicting arithmetic. Finally the experimental results in a single-phase half-bridge inverter demonstrate the good tracking control performances.

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