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A New Simulator for HVdc/ac Systems-Part II

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Abstract

This paper presents a performance comparison (the focus of numerical simulation) of traditional simulation (TCS,TSE) with an optimal step time simulator (SOST) for large HVdc systems.In SOST, a Detailed simulation of HVdc converter behavior has been modified to include the automatic selection of optimal integration steps, frequency-dependent effects of an ac system, ac system phase and magnitude dynamics of voltage (particularly weak ac systems), control assessment and temporary over-voltage consequences.

SOST, via graphical interfaces,provides fast and accurate information of electromechanical and the electromagnetic-transients behavior of a large HVdc/HVac system.

Key Words: *HVdc, Hybrid algorithm, Load flow, Dynamic behavior, Time domain analysis*

1. Introduction

Three conditions must be met for a rigorous approach to the problem of verifying of a computer algorithm:

1. Presenting all the relevant information needed to detect any deviations and the instances of their occurrence.
2. Setting up identical test system conditions in each model.
3. Comparing the proposed algorithm with one or more fundamentally different models.

A more realistic comparison [1,2], in terms of the conditions above, is the use of 3 or more alternative and fundamentally different computer solutions.

Three basically different approaches are currently used in HVdc/ac transient simulation, i.e. the electromagnetic transient program (EMTDC[3], EMTP), the hybrid algorithm (SOST, TSE (The hybrid concept of Transient stability (TS) studies and EMTDC) [4]) and the state variable technique (TCS [5]).

If the responses of the 3 methods (SOST, TSE and TCS) to various disturbances can be made to agree, it will be reasonable to accept their validity.

If they do not agree, at least one of them will not meet the criteria and without additional information it will be difficult to reach a positive conclusion as to the value of any of them.

The SOST [4] is based on a hybrid algorithm. The trapezoidal and backward Euler (critical damping method) rule is used to integrate the ordinary differential equation of lumped inductors and capacitors and convert them into a resistor in parallel with a current source, while lumped resistors are simply resistive branches.

Hence, a network of lumped R, L, C components is transformed into an equivalent circuit of resistive branches and current sources. Alternating current system components or valves are implemented by changing the value of the appropriate resistors.

For greater efficiency, SOST at power flow study and initial duration time of electromechanical stability with transient converter simulation uses the unified concept, which gives recognition of the interdependence of ac and dc system equations and simultaneously solves the complete system.

Further efficiency is obtained by using an optimal integration step time and frequency dependent electromechanical equation to reduce error and avoid numerical instability throughout the solution.

TCS [5] is a program specifically developed to analyze the dynamic behavior of HVdc systems and is formulated in terms of state space theory.

The behavior of the network in terms of branch currents and nodal voltages is determined by topological and algebraic constraints.

The instances of network topological changes or parameter value changes are determined accurately by changing the simulation step size (i.e. the lgorithm imposes no restriction on the integration step length).Inductance, capacitance and the like maintain their 'physical' form and remain constant within the integration step.

TSE utilizes Electromechanical Simulation as the steering program, and the electromagnetic-transients program is called a subroutine.

The interfacing code is written in separate routines to minimize the number of modifications and thus make it easily applicable to any stability and dynamic-simulation programs.

To make the description more concise, the component programs are referred to as TS and electromagnetic transient simulation EMTDC.

2. Test System

The dynamic comparison will concentrate on the HVdc converter, which constitutes the specific reason for the existence of TSE, TCS and SOST programs.

A realistic comparison of HVdc converter behavior provided by the 3 alternative algorithms can be achieved with reference to the simple test system illustrated in Figure 1.

The test system is an IEEE 9 busbars system. The line connecting busbars 4 and 5 of the system is replaced by a dc link, the characteristics of which are given in Appendix I. It consists of a monopolar dc link with a single bridge at each end provided with the basic control functions.

The reactive power loads of generator buses have not been considered.

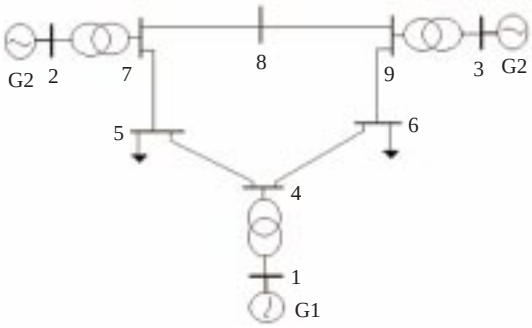

Figure 1. Test system.

3. Transient Behavior of the System

In this paper, due to space limitations, only the following tests are presented:

1. Initialization
2. Commutation failure at inverter

3.1. Steady state initialization

Prior to the dynamic comparison, it is necessary to start up the system from a de-energized state and observe the operating conditions under a steady state.

The steady state run was first used to identify and correct various anomalies in data preparation (per-unit systems) and information retrieval (elimination of zero sequence at converter voltages in the case of TSE and SOST). It was observed then that the 3 programs settled to the same operating point with a reference dc current of 456 A, a rectifier firing angle of 8.13° and an inverter extinction angle of 11.16°.

The entire valve conducting states changes took place with less than a 1° difference in the 3 programs.

3.2. Disturbance simulation-symmetrical and asymmetrical faults

Major disturbances in HVdc/HVac power systems lead to multiple commutation failures at inverters. Hence, for a credible validation, the 3 algorithms should produce the same pattern of commutation failures. In this section for symmetrical and asymmetrical faults full converter recoveries are displayed.

It is important that the switching be identified correctly, first for accurate simulations and second, to avoid any numerical problems rather than an inherent feature of the basic formulation.

A 50 Hz system simulated with a 50 μs time step has an average of 573 steps per cycle with the minimum requirement of 400 steps.

A 3 phase short-circuit of 2 cycles duration at bus 9 causing a 30% voltage reduction in the 3 phase (dc side current (Figure 2), ac voltage (Figure 3) and valve conduction times (Figure 4)).

A line-to-ground (L-G) fault, causing a complete loss of voltage in 1 phase of the receiving end ac system voltage was used to determine the highest TSE integration step needed to reproduce the performance of the SOST and TCS algorithms (50 μs for HVdc and ac system respectively) (the valve conduction times (Figure 5), dc side current (Figure 6), dc side voltage (Figure 7) and firing angles (Figure 8)).

The bar diagrams of Figure 4 and Figure 5 provide detailed information on the valve conduction times and with them a clear indication of commutation failure events, as a result, the converter recovery following

fault clearance of 3-phase short circuit is exactly the same in the 3 cases, but for a line-to-ground fault, small differences are now observed.

For instance, valve 1 has one conduction period at 0.519 s in SOST, which is totally absent in the TSE simulation. The above differences in valve conducting patterns in asymmetrical cases are not due to differences in controller outputs, which have been ensured to be the same (Figure 5b) particular instants and, therefore, they must be due to differences in the algorithmic efficiencies.

The SOST algorithm[6] imposes no restriction on the integration step length, and the instances of network topological changes or parameter value changes are determined accurately by changing the simulation step size.

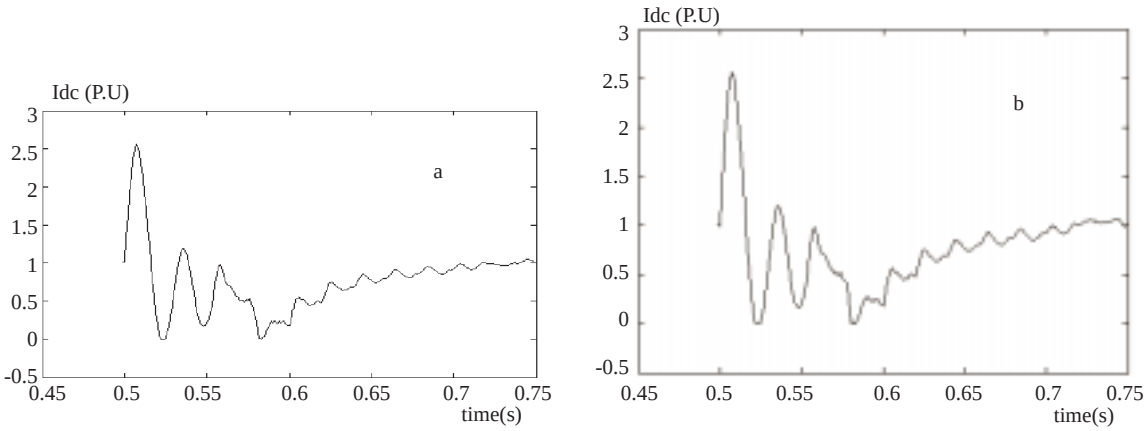

Figure 2. Three-phase fault at the inverter end The dc side current a)SOST b)TSE.

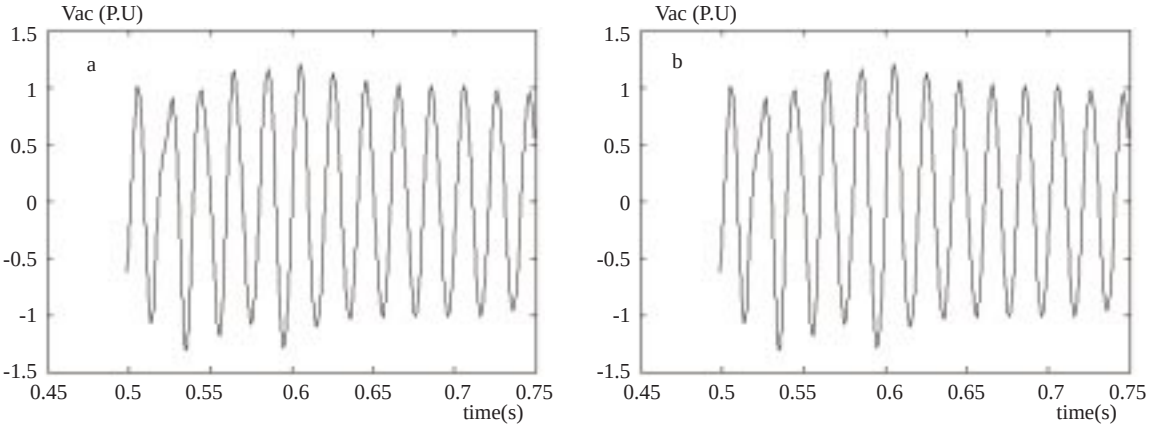

Figure 3. Three-phase fault at the inverter end. Rectifier ac voltage a) SOST b) TSE.

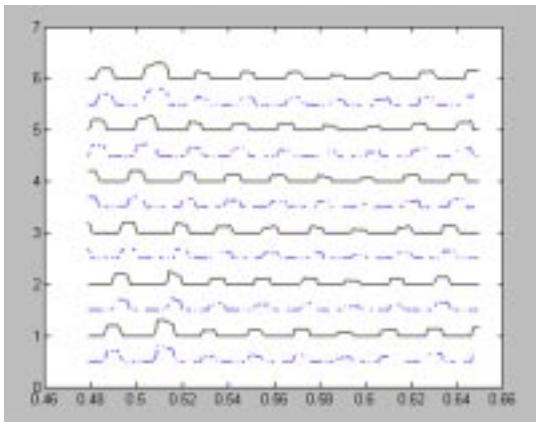

Figure 4. Three-phase fault at the inverter end (valves conduction).
—— TSE,
- - - SOST

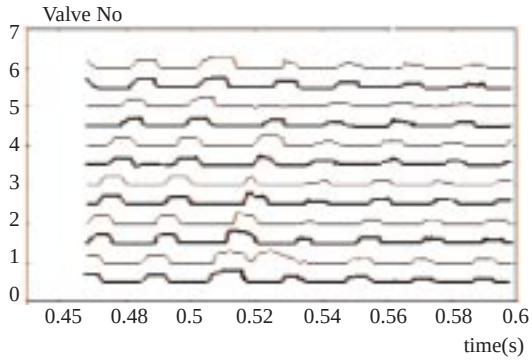

Figure 5. Valves conduction, a: controller outputs, b: valve current.
—— TSE,
- - - SOST

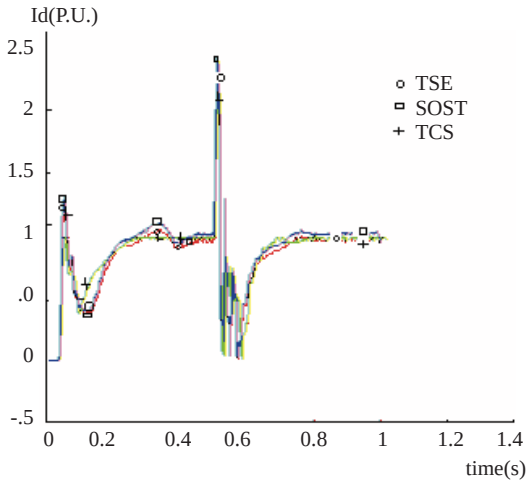

Figure 6. The dc side current (L-G).

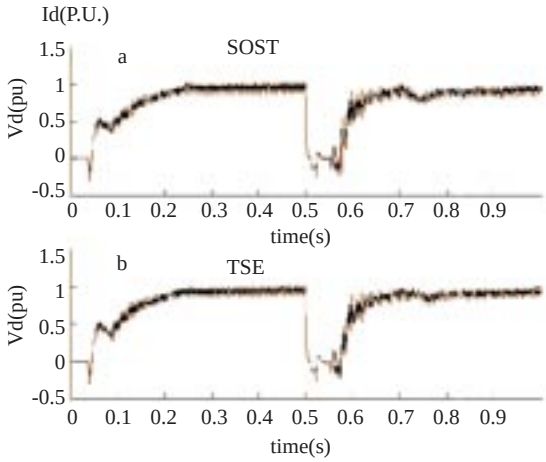

Figure 7. The dc zide voltage (L-G).

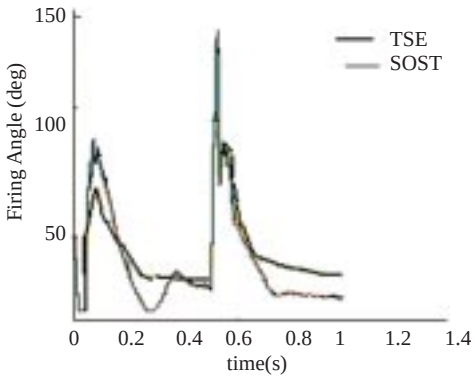

Figure 8. Firing angles (L-G).

The time for switching 'ON' a converter valve and fault application is easily determined before the event.

The time of zero current in converter valves and fault branches is detected after they occur and the optimal step time algorithm is used to derive the switching instant [6], the TSE considered acceptable to run EMTDC for a full period without updating the system 1 equivalent circuit during fault time.

Sequential numbering in Figure 9 explains differences ir the flow of events between SOST and TSE.

Although the above concept has some advantages, it also suffers from many disadvantages, in particular, for weak ac systems Table 1 depicts the ac voltage at bus 4 and 5 after 3-phase faults at bus 9 (waveform distortion is also likely to be significant).

Table 1. Dynamical response 3-phase faults (Voltage < angle).

T(s)	BUS 4(p.u)	BUS 5(p.u)
0.50005	0.80068 < -2.263	0.71483 < -28.8
0.50010	0.80052 < -2.241	0.71362 < -29.02
0.500150	0.80041 < -2.229	0.71297 < -29.19
0.500200	0.8003 < -2.217	0.71233 < -29.35
0.500250	0.8002 < -2.205	0.71170 < -29.5
0.5003	0.8001 < -2.193	0.71108 < -29.65
0.50035	0.8000 < -2.182	0.71047 < -29.8
0.50500	0.94902 < -1.434	0.92037 < -33.93

Electromechanical steady-state step lengths: 0.0005 [s]

4. Implementation of Optimal Step Time Algorithm

The optimal step time algorithm is not a replacement for chattering removal and interpolation. but a complement. Tables 2, 3 show simple examples of the optimal step time algorithm (if N > 800 then k = 1 and analytical and optimal step time (OST) responses are practically identical).

Table 2. Sampling function.

a) $\dot{\psi}_1 = -\psi_1 A$ b) $\dot{\psi}_1 = -1 - \psi_1 A$

$\dot{u} = u$	$\dot{u} = e^t$	
e^t	e^t	Analytical response
1	0	A=$\frac{\partial f}{\partial u}$
e^t	1	$a = e^{\int_0^t Adt}$
e^{-t}	1	$\Psi_1 - (a$
$\frac{e^T - e^t}{e^t}$	T-t	$\Psi_1 - (b$
$\frac{1}{2}e^t$	$\frac{1}{2}e^t$	$E = \frac{1}{2}\left(\frac{\partial f}{\partial t} + ...\right)$
$\left(e^T - e^t\right)^{-\frac{1}{2}}$	$\{(T-t)\,e^t\}^{-\frac{1}{2}} e^{-\frac{1}{2}}$	h(t)

At the fault time (Figure 9), unified electromechanical HVdc/HVac system is called for a length of fundamental period (arrow 1)and the interpolation method over this full fundamental period is given back to unified electromechanical ac/dc at time t (arrow 2),and runs to t + T (arrow 3),using equivalent-circuit information derived for that particular time step (arrow 4).

Table 3. Comparison between SOST and analytical method.

N	$u_{o.s.t.}$	$\delta u_{(u.s.t.)}$	$\delta u_{(\text{analytical})}$	K
100	8.512416	1.870178	1.487584	1.2572
200	9.172265	0.827735	0.935089	1.1297
400	9.561057	0.438943	0.467544	1.0652
800	9.773621	0.226379	0.233772	1.0327

$$K = \frac{\delta u_{(o.s.t.)}}{\delta u_{(\text{analytical})}}$$

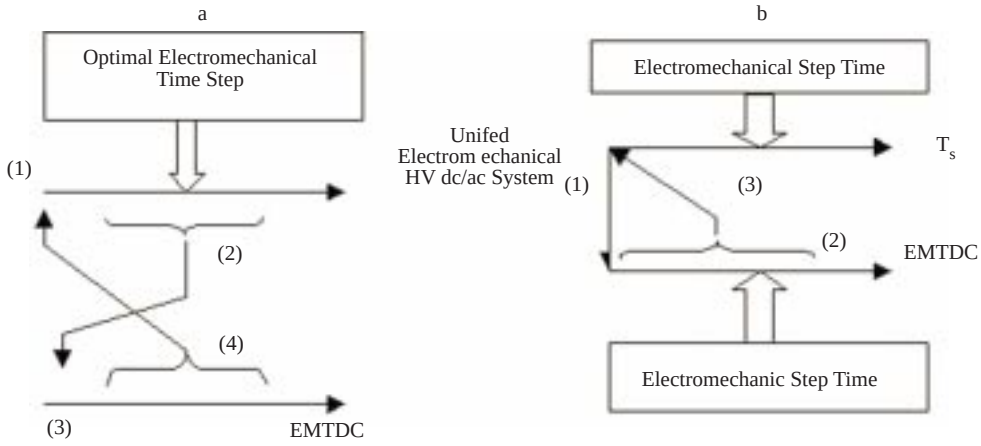

Figure 9. Differences the flow of events between SOST and TSE a) SOST, b) TSE.

5. Computing Times

For the test system with 3-phase short circuit fault and a 1[s] simulation run, and 50 μs step time, the total computing times in a Pentium (r)II processor Intel MMX, 128.0 MB RAM computer were as follows:

Table 4. Computing times.

	Time[Second], (3-phase fault)
TSE	26
SOST	22
TCS	22

6. Powerflow Study (sequential method)

Power flow study in SOST is based on the unified method. The overall convergence rate of the ac/dc algorithms depends on the successful interaction of the 2 distinct parts. The ac system equations are solved using the well-behaved constant tangent fast decoupled algorithm, whereas the dc system equations are solved using the more powerful, but somewhat more erratic, full Newton-Raphson approach for dc equations, which can cause overall convergence difficulties.If the first dc iteration occurs before the reactive power voltage update, then the dc variables are converged to be compatible with the incorrect terminal voltage. This

introduces an unnecessary discontinuity which may lead to convergence difficulties in the sequential method (Table 5).

Table 5a. Number of iteration for test system (strong ac system)- (Q: reactive power control, P: active power control).

m-rectifier, n-inverter	SOST (Unified)	Sequential P, Q, DC
A mPdmγnVdn	3	5
A mPdmanVdn	4	6

Table 5b. Number of iterations for test system (weak ac system) - (γ, α: extinction, firing angle control).

m-rectifier, n-inverter a: tap	SOST (Unified)	Sequential P, Q, DC
A m PdmγnVdn	3	3
A m P manVdn	4	6
A m P dm anVdn	>5	5

7. Experimental Results

The experimental test system is a 6-pulses HVdc/ac system with ac voltage 380 V(voltage during the test is unbalanced (190 < 0, 212.5 < -121.1, 202 < 123)),thyristor valve(SKT50, ignition angle for rectifier = 40°, and for inverter is 132°) single phase transformer in rectifier side (Rt = 1.58 Ω,Lt = 0.96 mH), and 3 phase/3 limbs transformer in inverter side (Rt = 1.02 Ω,Lt = 0.86 mH), the snubber circuit (r = 100 Ω, c = 0.22 μf) for each valve is included in the model dc inductor is 0.498 H and dc resistance is 2.797 Ω.

Figures 10 (dc current), 11 (primary phases current transformer) and 12 (secondary phases current transformer) show oscillograms (experimental results) obtained from the test of the HVdc/ac converter and simulated results by SOST.

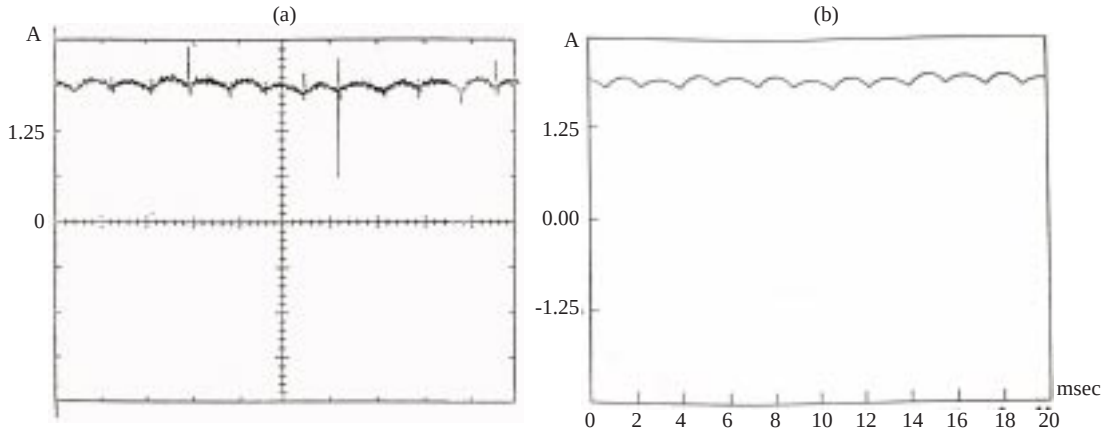

Figure 10. The dc side current a.experimental results, b. simulated results.

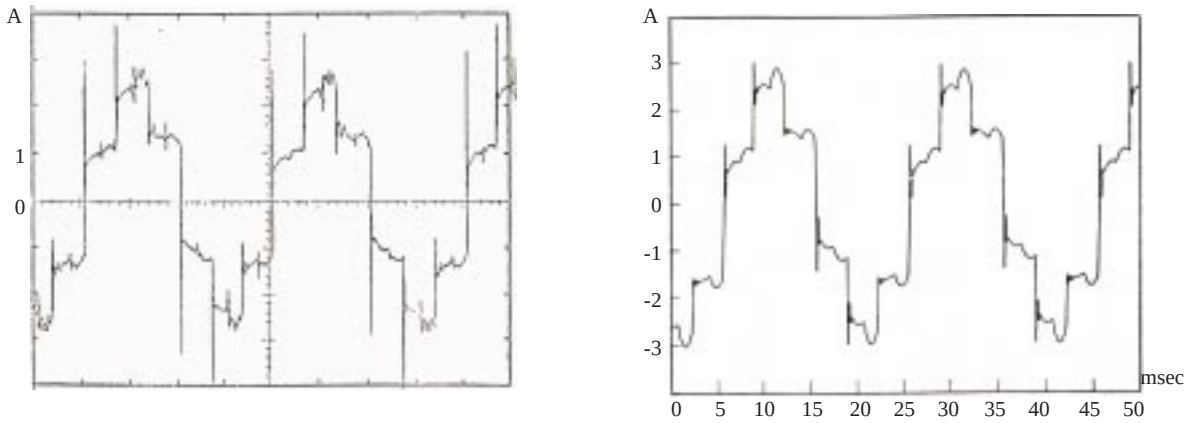

Figure 11. The secondary phase current transformer a. experimental result, b.simulated result.

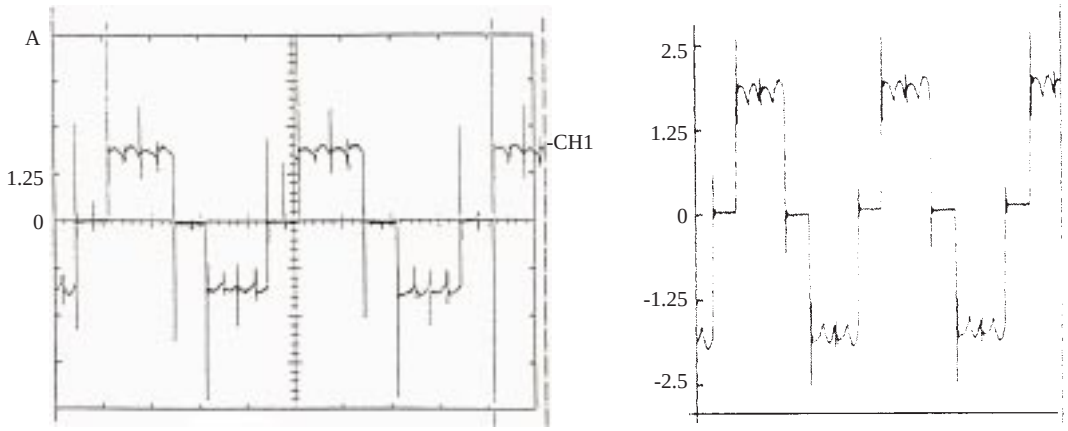

Figure 12. The primary phase current transformer a. experimental result , b. simulated result.

8. Conclusions

The TSE algorithm has been modified to include the automatic selection of optimal integration steps, frequency-dependent effects of an ac system, root matching techniques, ac system phase and magnitude dynamics of voltage (particularly weak ac systems),control assessment and temporary overvoltage consequences.

To demonstrate the advantages of the hybrid solution, 2 different disturbances (symmetrical and asymmetrical faults) have been applied to a simple test system.

First, a 3-phase fault at the inverter-converter terminal to validate the hybrid technique by showing that the response is practically identical to that of TSE programs.

Line-to-ground fault at the inverter-converter terminal exemplifies the differences between the 2 types of solution. The SOST algorithm, though reputed to be efficient, uses fewer approximations and provides automatic selection of optimal integration steps. After the fault has been applied TSE is considered to run EMTDC for a full period without updating the system 1 equivalent circuit during this time. However, SOST is considered to run electromechanical stability system for a full period and the interpolation of results over the full period is processed and passed back to update the system 1 equivalent in EMTDC; however, some deterioration occurs with highly asymmetrical disturbances (ac voltage are greatly destroyed after faults acquired).

The results show that where the ac system is weak, the power flow study(sequential algorithm) is susceptible to convergence problems and if the ac system is strong the unified algorithm may be programmed to give fast and reliable convergence. Thus in general, the unified method is recommended due to its greater reliability.

Our comparison between experimental and simulated results shows SOST to be very efficient and accurate.

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Appendix 1

Table 6. Line data of 9 busbars power system and dc link.

Line	Busbar	R(p.u)	X(p.u)	B/2(p.u)
1	1-4	0.0000	0.0576	0.0000
2	4-5	0.0100	0.0850	0.0880
3	4-6	0.0170	0.092	0.0790
4	5-7	0.0320	0.1610	0.1530
5	6-9	0.0390	0.1700	0.1790
6	2-7	0.000	0.0635	0.0000
7	7-8	0.0085	0.0720	0.0745
8	8-9	0.0119	0.1008	0.1045
9	3-9	0.0000	0.0586	0.0000

	Rectifier	Inverter
Bus number	5	4
Commutation reactance	0.126	0.07275
Minimun control angle	7	10
Transformer regulation range	15%	15%
Number of tap positions	27	19
Filter admittance	0.4002	0.6301
Resistance of the dc line	0.00334	
dc power flow setting	0.5857	
Inverter end dc voltage	1.284	