The Future of Gold in Electronics

Timothy W. Ellis
Principal
Triaxial Structures Inc.
Philadelphia, Pa, USA

Gold-based materials have been a mainstay of the electronics and semiconductor industry since the physics was just a laboratory curiosity. Gold is the workhorse material in wire bond, flip chip and off wafer interconnections due to its corrosion resistance, ability to form metallurgical bonds by soldering or cold welding, and ease of fabrication. As the electronics and semiconductor industries grew, so did the use, of gold in spite of the feature size reduction so elegantly demonstrated in Moore's law. However, several revolutions in the Silicon miracle are threatening gold's place as the material of choice. Although cost is always an issue, the limitations are associated with the chemistry of gold based alloys. Will gold remain? Emerging requirements of bioelectronics, photonics and power requirements in conventional device represent new opportunities for gold to shine. Additionally, as the world market demand for electronic, semiconducting, bio-electronic and photonic technology increases, given the right technology, gold still can provide value proposition.

Introduction:

On inspection of the keynote address for the Gold 2003 Conference, I was struck by the fact that all of the topics to be presented had a high probability of showing up in or on electronic devices. I believe this dramatically demonstrates the intimate relationship between the electronics industry and Element 79.

Gold (Au) metallurgy has been a core enabling technology in the research, development and production of electronic devices. In 1786 Englishman Abraham Bennet invented the gold-leaf electroscope, Figure 1, (1), which was probably the first modern use of gold in an electronic device. Although we can safely assume gold was used by Thales, the Greek philosopher, to experiment with static electric charges generated by amber as early as 6000 B.C., gold was used in the ever-increasing array of scientific instruments revolving around electrical phenomena as the industrial revolution progressed. The physical properties that made gold the metal of choice then still drive its use in present electronic devices and packaging.

The Solid State Revolution

The first solid-state transistor, Figure 2, was tested on December 12, 1947 at ATT Bell Laboratories in Murray Hills New Jersey (2). As reported by John Bardeen, the discovery revolved around gold: "In fact the device worked as if there was no oxide layer at all. And as Brattain poked the gold contact in again and again, he realized that's because there wasn't an oxide layer, he had washed it off by accident. Brattain was furious with himself, but decided to fiddle with the point contact anyway. To his surprise, he actually got some voltage amplification — and more importantly he could get it at all frequencies! The gold contact was putting holes

Figure 1
A gold leaf Electroscope

Figure 2
Photo of the First Successful Solid State Transistor

into the germanium and these holes cancelled out the effect of the electrons at the surface, the same way the water had. But this was much better than the version that used water, because now, the device was increasing the current at all frequencies". The ability of gold to supply holes arguably allowed a useful solid-state device to be recognized very early in the Bell Labs work.

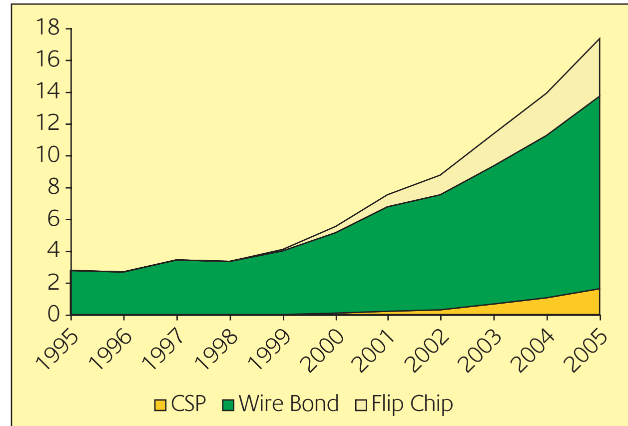

Figure 3
Growth of Semiconductor Interconnects, in billions of units

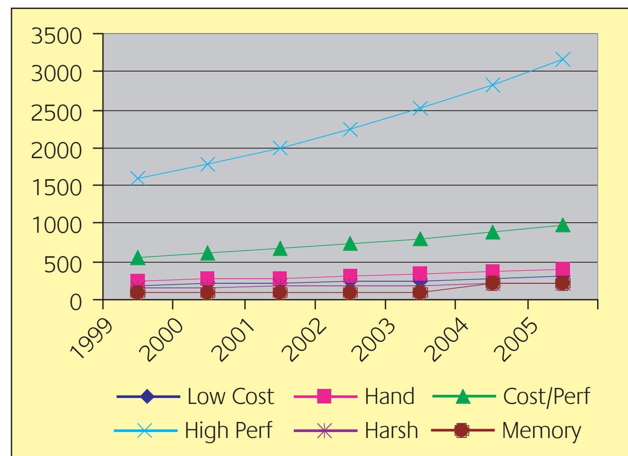

Figure 4
I/O Count versus Package Type 1999 – 2005, from ITRS Roadmap (3)

Present Limitations

Economics of the Electronics Industry

The economics of the electronics industry is brutal. Decades of double-digit growth enforced fast globalization, as electronic capability strained to keep pace with human creativity and a demand for evermore electronified life styles. What drives the consumption of gold in electronics? The numbers of devices and interconnects in the electronics industry is staggering by all measures. Trillions of interconnects are made each year and gold is key. Gold as wire and as bond pad metallization on packaging accounts for the significant share of the electronics industry's utilization of gold based alloys.

The growth in electronic interconnects over the decade 1995 to 2005 is shown in Figure 3. Even given the slow down of 2000 – 2003, the decade may post a 9-fold increase in the number of interconnects (3). However, the growth in the number of interconnects is not uniform. Though the ultra high end CPU's, DSP's, graphics and voice processors are growing I/O (Input/Output) count dramatically, a great deal of the industry still has a relatively modest I/O count, Figure 4. A poignant aside is that the high I/O count market has made a significant transition from wire bonded package with micron scale gold wire to Flip Chip processes with sub-micron gold bond pad coatings.

The corollary to the I/O growth curve is that the cost per I/O is dropping rapidly, Figure 5: at the high end the cost of an interconnect can be high, as the value of a CPU, for example, is relatively high. However, in the volume, bulk low I/O market, the cost of interconnection is not an insignificant portion of the finished device cost; as such the pressure to drive to lower cost; is dominant. This cross current of the loss of high I/O packages and intense cost pressure at the lower I/O count may reduce margins in the gold wire business to unacceptable levels.

What is the ramification to the consumption of gold in electronics? The use of gold is mainly as wire for wire bonding which is still the predominant semiconductor packaging process. As can be seen in Figure 6, using data from the ITRS road map, the volume of gold wire per package is going down dramatically

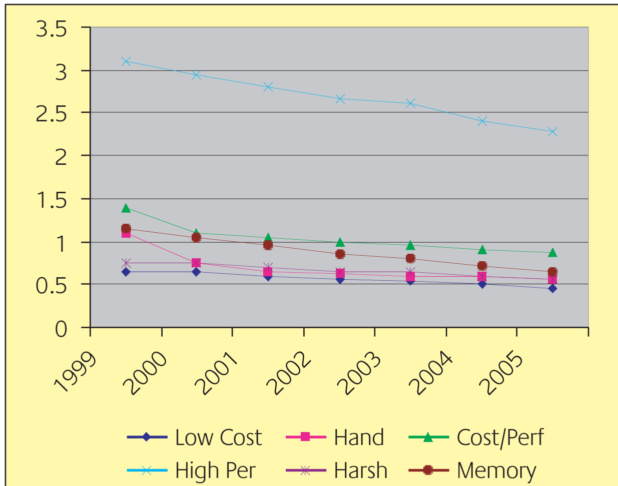

Figure 5

Cost (Cents)/Pin for Various Package Types, 1999 – 2005, from ITRS Roadmap (3)

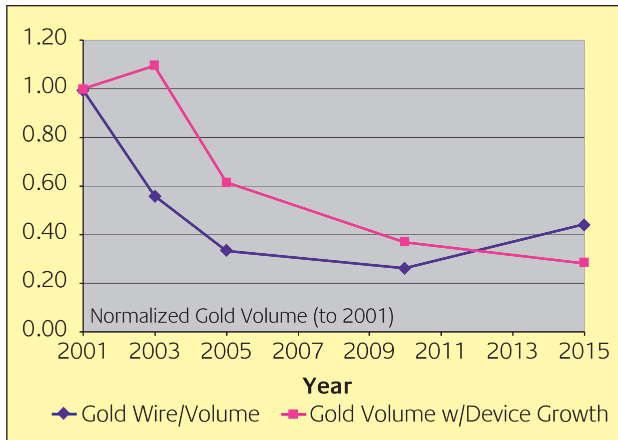

Figure 6

Volume of Gold Consumed by Wire Bonding Calculated for Pitch Reduction and Production Volume Increases. (3)

due to the reduction in wire diameter, in leading edge process, from 25 microns (2001) to 10 microns (2010) (3). The reduction in gold wire by the square of the diameter is not being compensated for by the 9.8% increase in global semiconductor growth, calculated by Mike Vinson of the American Competitiveness Institute. One can also question whether the turn up in 2010 will actually occur as the volume upturn is caused by the stagnation of wire diameter at 10 microns, allowing device volume to catch up. Without questioning the ability to produce 10 micron wire in volume and its use in real industrial processes, the transition to Flip Chip with the concomitant reduction in gold consumption from wire to flash plating would seriously challenge an upturn in consumption.

Gold Intermetallic Failure Mechanisms

Gold intermetallic compounds are to be found in over 90% of the electronic interconnections. In wire bonding, understanding the Au – Al binary system is key while soldering attachments in Flip Chip or Printed Circuit Board assembly. Gold pad coatings assure high quality assembly processes using Pb – Sn or Pb-free solders. With the Pb–free mandate, a wide variety of micro-additions, e.g. Sb, Cu, Ag, Bi, are also coming along and need to be considered. Although the formation of intermetallics thermodynamically drives bond formation, they can also be brittle or cause voiding due to unequal diffusion effects. The development of fracture, voids and stress gradients due to intermetallic formation is leading to assembly issues which challenge gold's dominant technical position.

Over the last several year's, conventional Au-Al wire bonding metallurgy has developed reliability issues which calls into question its further usefulness for off-chip interconnect. The issue is summed up very simply in the phase diagram presented in Okomoto and Massalski "Phase Diagrams of Binary Gold Alloys" (4). Specifically pay close attention to the study by Vanderberg and Hamm on the

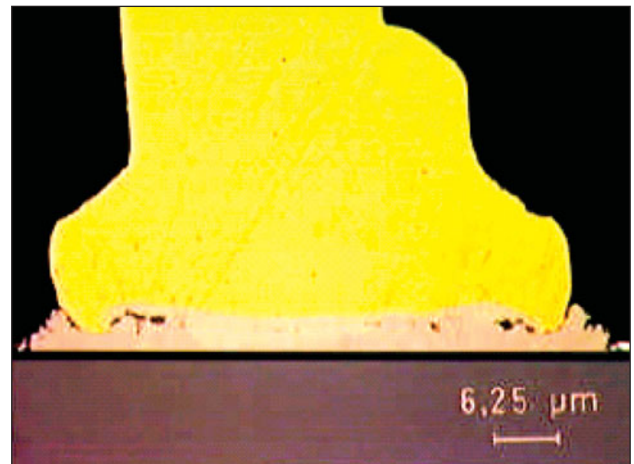

Figure 7

Cross-Section of an Au - Al Ball Bond Aged @ 175C for 1000 Hrs

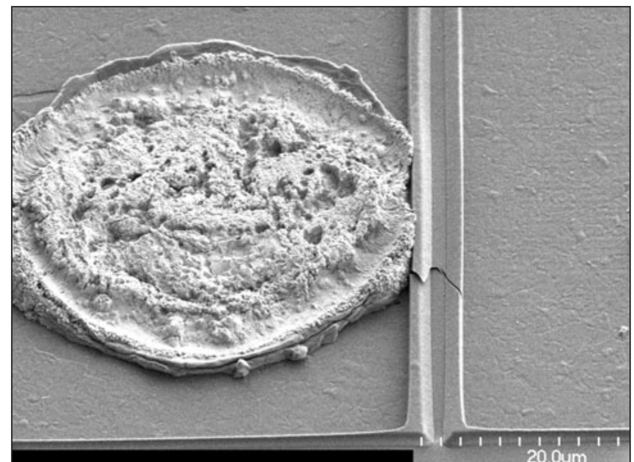

Figure 8

Lifted Au - Al Ball Bond Produced by Aging @ 175C for 1000 Hrs

phase selection found upon aging sputtered Au-Al films (5). By inspection, we can see that, at approximately 160°C, the phase selection of intermetallics in the Au – Al system changes with the development of the Au_4Al phase. Previously unpublished research by the author has shown that the temperatures above 160°C produce an unacceptable failure rate due to void formation and interface fracture. Although outside the scope of this paper, modeling studies have shown one possible mechanism is intermetallic formation, which leads to volumetric expansion differences and the creation of large differences in diffusion-driven mechanical stress gradients. Figures 7 and 8 are cross section and lifted aged Au - Al bonds showing the formation of voids and interfacial fractures. Since the diffusional processes that form the intermetallic layer are independent of the bond size, these defects are found to be more detrimental when squashed balls are smaller than 50 microns. Unfortunately, to support high I/O advance devices, a small bonded ball size is required to physically fit all the necessary interconnections on the die.

Whiskers of tin have again become a problem in electronics with the legislated march toward Pb–free interconnection alloys, Figure 9.(6) Unlike dendrites, whiskers are thought to grow by vapor transport or to relieve stresses in the tin due to crystallography.

Although still a subject of research, intermetallic compound formation has been found to affect the nucleation and growth of tin whiskers in application. Since gold forms intermetallics with tin and essentially all of the alloying elements present which have also been shown to impact whisker formation, e.g. Ni, Cu, Au, Pd, this may also lead to changes in the use of Au as a bond pad material in Pb-free applications.

Emerging Opportunities

Direct Write Processes

The increased functionality of present semiconductor devices places extraordinary demands on device packaging.

Figure 9
Example of Tin Whiskers (20)

Unfortunately for the semiconductor and electronics assembly industries, the process used to package devices has not kept up with Moore's law. This is true for both the speed of interconnect rate and density. Assembly processes still consist of: (i) ThermoSonic Welding, manifested by Wire or Tab Bonding, (ii) Liquid Metal Joining, i.e. soldering, demonstrated in Flip Chip packaging and PC board assembly, and (iii) Polymer Filled Adhesives, essentially metal-filled epoxies which are used in a Flip Chip type operation Substrates are still essentially produced by photo-etching techniques; these are rather limited options given the requirements for device performance and cost. These choices are still the same that started with the industry over 50 years ago.

Research into Direct Write technologies have some opportunity to move beyond the limits present in assembly technology. The compilation of direct write technology by Pique and Chrissy (which is centered on the DARPA MICE program, Mesoscopic Integrated Conformal Electronics), is a notable reference in the area (7). The ability to directly write metallic lines <20μm width would open up a whole new realm of packaging possibilities. Incorporation of integrated passive devices, i.e. capacitors, resistor, inductors, in the package structure during assembly would allow greater design flexibility and, presumably, lower cost by eliminating individual assembly steps. Lead-free joining operations, i.e. soldering, replaced by gold metal deposition at specific joint locations would be thermally and environmentally more friendly. Present lead-free solder, usually tin-based, requires higher reflow temperatures than conventional leaded solders. High temperature, 260°C reflow, can be very damaging to the organic-based built-up multilayer boards in packaging. A completely new low temperature approach, based upon gold's chemical properties, to flat panel/board integration with quick assembly processes re-tooling can be envisioned, given a direct write process. This would free the electronics package designer to build more compact and logically less expensive devices by the simple elimination of assembly process steps and re-tooling/qualification expense. However, to be viable in the electronics assembly world, several challenges need to be overcome as devices and packaging are moving down a very steep cost-performance curve. Assembly processes and materials need to intersect the ITRS roadmap +2 years out from commercialization to give users time for manufacturing development. Direct write, based on gold metallurgy, would need to demonstrate technological headroom, keeping pace with future requirements of the industry, even to be considered but a lack of other options does open a window of opportunity.

Nano-Electronics, Sensors, MEMS and Optoelectronics

Gold films for interconnections, absorption substrates, electrodes, quantum dots, or single atom tips are the mainstay of the nano-electronics revolution (8). The fabrication of nano-clusters, accomplished by using STM procedures, was demonstrated by Kold, Ullmann and Will (9). On the complete opposite tack, self-assembly processes, using gold, have been extensively studied and thought key to large scale production of nano-technology at a market acceptable price (10). Coupled with the ability of gold to be used to develop nano-patterned surfaces using alkanethiols (11), self-assembly has been extended to developing metal/organic interfaces by Groves, Ulman and Boxer, who constructed micro-patterned lipid bilayers upon a substrate patterned with Au, Al_2O_3 and SiO_2(12). A direct write process, by stylus writing, has successfully been used at Northwestern University by the group lead by C. Mirkin to construct patterns (13). Studies by Chen *et. al*. have shown that gold nano-particles can through size control be manipulated from a metal to a molecular-like bonding which allows the electrical properties of the interface to be tailored between metallic and covalent bonding (14). The combination of the work described here shows that the technology to produce electronic surfaces, where organic molecules are bonded to metallic conductors, takes advantage of the chemistry of gold.

MEMS technology is heavily dependent upon gold metallurgy. Gold is commonly used as a plating for hermetic packages to allow for sealing and prevent corrosion, i.e. tungsten carriers. This is a heritage derived from common telecommunications and Optoelectronic packaging practice. This should be expected, as many of the first applications of MEMS technology have been in the telecommunication market. By definition, MEMS devices have active mechanical parts that are susceptible to failure due to contamination fouling the works. Also, since many MEMS-based devices are for industrial/commercial infrastructure, the time in service and reliability requirements are above those for more consumer-driven applications (15, 16). Nano-device production methodologies such as LIGA and Micro-Print also use gold plating and coating technology to transfer the soft polymer based structure into hard engineering materials (17, 18). This technology has been expanded to the development of actuators, where gold can serve as an environmental coating, electrode or substrate upon which an electroactive polymer or molecular species is deposited. (19).

Advanced semiconductor technology for solid-state lasers, high-powered diode and power electronics will need to use gold-based materials. These devices, e.g. based on SiC, GaN, GaAs, AlGaN, operate at elevated temperatures and high electrical currents; therefore, gold is used to prevent oxidation and provide a thermal contact pathway (19).

Conclusion

Gold has been key to the development of the modern electronic world we all enjoy. Gold continues to be an enabling material for the development of emerging Nano, MEMS, and optoelectronic technologies. The question of where the troy ounces will come from is unclear however. Cost is the over-riding consideration in the market it drives, the applications and the adoption of new applications. As such, the volume of gold use will remain under pressure simply to keep driving down the cost curve. Gold will dominate where no other material will perform the application at a lower cost. If gold does not, it will be replaced by a more cost-effective solution. So gold utilization in electronics will be dependent upon new technologies coming to the market at a faster rate than gold loses share in pre-existing production.

About the Author

Dr. Ellis has focused his career on the “Science to Money” problem, the transitioning of laboratory results to products. Presently Dr. Ellis and several colleagues are engaged in developing a business development firm around small capital company. Dr. Ellis, in addition to his engineering degrees from Michigan Tech and Iowa State, has a masters in Technology Management from the University of Pennsylvania.

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