

Gold in Silicon: Characterisation and Infra-red Detector Applications

Leonard Forbes

Department of Electrical Engineering, University of California at Davis, Davis, California, U.S.A.

Gold is used as a deep level impurity in silicon in semi-conductor devices. In this paper the characteristics of the gold impurity centre are reviewed, an almost complete characterisation having been achieved by the indirect observation of its charge states in space-charge regions. The application of gold-doped devices as infra-red detectors is also discussed.

Gold is a double level impurity in silicon (1, 2), introducing both an acceptor level and a donor level in the band gap, as shown in Figure 1, between the conduction band and the valence band. The designations donor and acceptor refer only to the possible charge states of the impurity centre; donors can have neutral and positive charge states and acceptors can have neutral and negative charge states.

The impurity centre can change charge states in the semi-conductor only by the emission of carriers either to the conduction or to the valence band and the capture of carriers from one of the bands. Figure 1 shows six of the possible processes for gold in silicon, where the letter "e" indicates an emission process and the letter "c" a carrier capture process. The first subscript gives the type of carrier involved in the process; "n" is electron and "p" is hole. The second subscript gives the initial charge state of the impurity charge state in terms of the number of negative electronic charges present. "C_{pl}" for

instance is hole capture at negative gold. The donor state for instance can change from a positive charge state by the emission of a hole or a positive charge to the valence band and can change from the neutral to positive charge state by the capture of a mobile hole from the valence band. Likewise the acceptor state can change between negative and neutral charge states by the capture and emission of electrons and holes from the valence or conduction band as appropriate. Capture and emission of electrons by the donor state are not shown, since they are relatively unimportant here.

A knowledge of the energy differences involved in these processes, and the rates of the processes, in what is known as the Shockley-Read-Hall model would constitute then a complete characterisation of the impurity centre allowing a description of the effect of gold-doping on any silicon semi-conductor device (3).

Such an almost complete characterisation has been

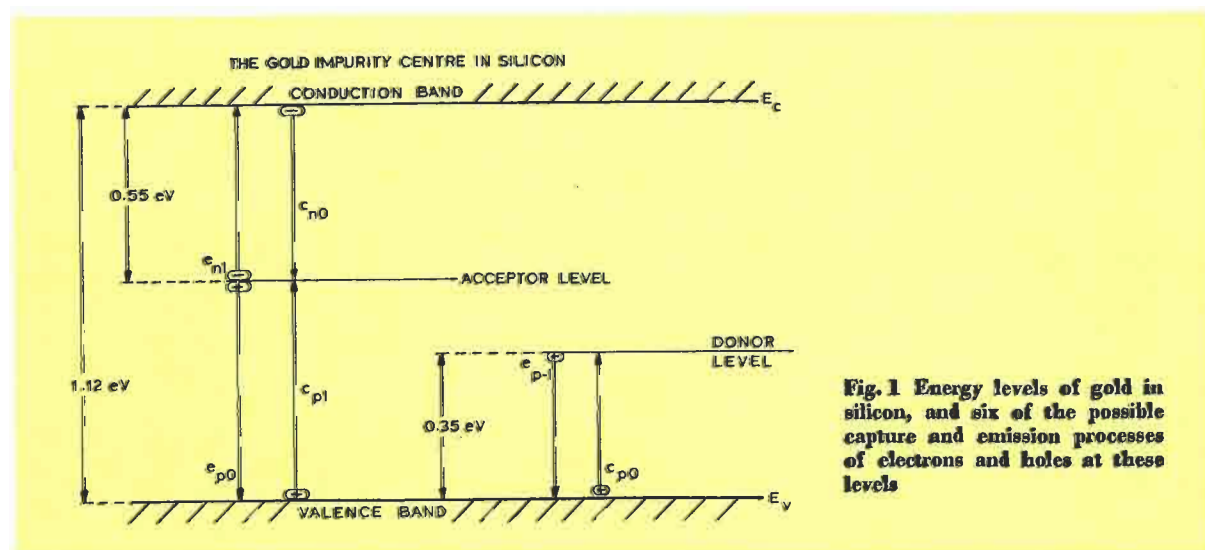


Fig. 1 Energy levels of gold in silicon, and six of the possible capture and emission processes of electrons and holes at these levels

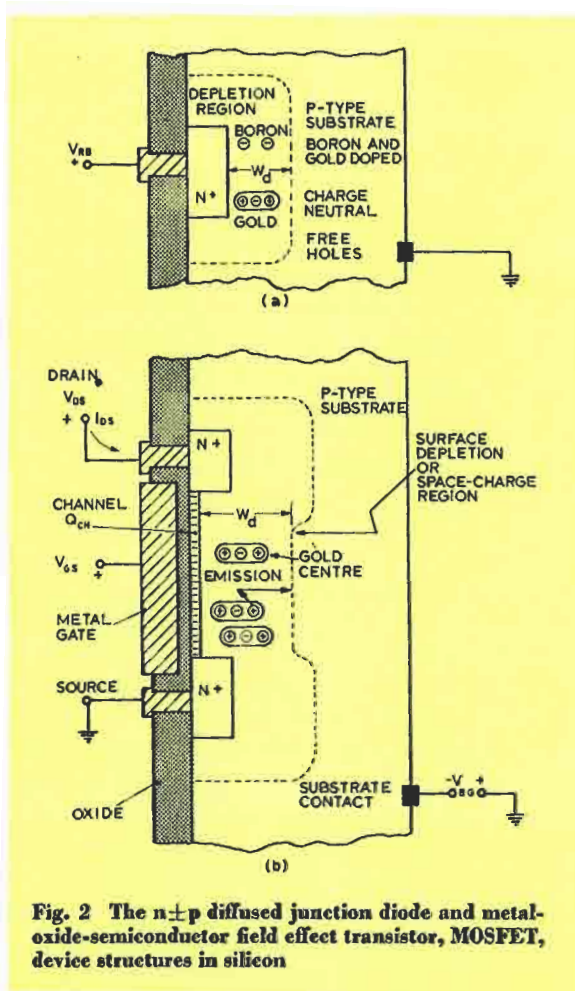


Fig. 2 The $n \pm p$ diffused junction diode and metal-oxide-semiconductor field effect transistor, MOSFET, device structures in silicon

achieved for the gold impurity centre in silicon by the indirect observation of these changes in impurity charge states in the depletion regions of silicon semiconductor devices, including p-n junctions and metal-oxide-semiconductor (MOS) device structures (4-7).

Characterisation Techniques

Figure 2 shows some of the semiconductor device structures that have been used in the characterisation of gold in silicon. Figure 2a shows the $n \pm p$ diffused junction and Figure 2b the n-channel metal-oxide-silicon field effect transistor structure, MOSFET. These device structures have associated with them a depletion region, or a region in which there are essentially no free or mobile carriers when a reverse bias, V_{RB} , is applied to the $n \pm p$ junction or a reverse bias, V_{BG} , is applied to the substrate contact of the MOSFET device structure. The objective of observing the change of charge state of the gold impurity centre in a depletion region is to enable the observation of a single process, either capture or emission. In all techniques employed in the past, as the Hall effect or photoconductivity (1,2,8), more

than one process occurs, greatly complicating the interpretation of the experimental measurements aimed at characterising the centre.

In normal circumstances then in a depletion region of a device structure there are no free carriers available to be captured by the impurity centre, and the only way the centre can change charge state is by the emission of carriers. Consider the case of the $n \pm p$ junction: if the gold impurity is arranged to be initially in the positive charge state then it can change to the neutral charge state by the emission of a hole from the donor level to the valence band and the hole will be swept out of the depletion region by the electric field in this space-charge region. The gold centre can be arranged to be initially in the positive charge state by applying zero bias to the junction, allowing the depletion region to collapse and ensuring a large hole concentration in the vicinity of the gold impurity centre and consequently a positive charge state. When the reverse bias is applied to the junction the gold will change charge states from positive to neutral.

If the reverse bias is held constant during this time then the change in gold charge state will result in a modulation of the space charge concentration on the right-hand side of the junction. The total amount of charge on the right-hand side of the junction depletion region and the applied potential are not, however, independent and determined by Poisson's equation; if the applied potential or bias is fixed then to first order, the total amount of charge is fixed. If the charge concentration changes due to positively charged gold becoming neutral this can be accomplished only if there is a change in the width of the depletion region, W_d . In the $n \pm p$ junction the change in width of the depletion region will result in a change in the high frequency capacitance of the junction, which is given by the parallel plate capacitor formula, $C_{HF} = K_s \epsilon_0 / W_d$, where K_s is the dielectric constant of silicon. In the MOSFET device structure the change in the depletion region width will result in a change in the drain-to-source current, I_{DS} .

By observing the time constant associated with the change in the high frequency capacitance or time constant of the change in drain current one can determine the emission rate, e_{p-1} , which is simply the reciprocal of this time constant. If there is no external excitation, by infra-red radiation, the only means by which the hole can gain the required energy to escape is from the thermal energy associated with the silicon lattice vibrations. This is then the thermal emission rate which can be expressed as

$$e_{p-1}^t = A \exp(-\Delta E/kT)$$

where ΔE is the energy difference involved in the process and T the temperature (4, 9, 6).

By measuring the temperature dependence of this

emission rate one can not only determine the thermal emission rate itself but also the energy difference, ΔE , in this case between the valence band and donor level. This provides a unique means of locating the energy of the donor level in the band gap of silicon. Similar experiments can be done on $p \pm n$ junctions and the energy differences and rates involved in electron and hole emission from the acceptor level determined. These results are shown in Figure 3, where the energy differences involved have also determined the location of the acceptor level in the band gap as shown in Figure 1 (4, 9, 6).

Once known, not only can this information be readily used to provide a unique identification of small residual concentrations of gold impurities in an unknown sample, but it can also be used to determine very accurately the value of the concentration of gold in purposefully doped devices (5).

As shown in Figure 3, the thermal emission rates become very small at low temperatures and this fact can be used in the construction of very sensitive infra-red detectors. If a gold-doped device is cooled to a very low temperature, then thermal emission is eliminated as a means for the impurity to change charge state. The carriers trapped at the impurity centre can, however, gain sufficient energy from external illumination by an infra-red source to escape from the attractive potential of the impurity centre;

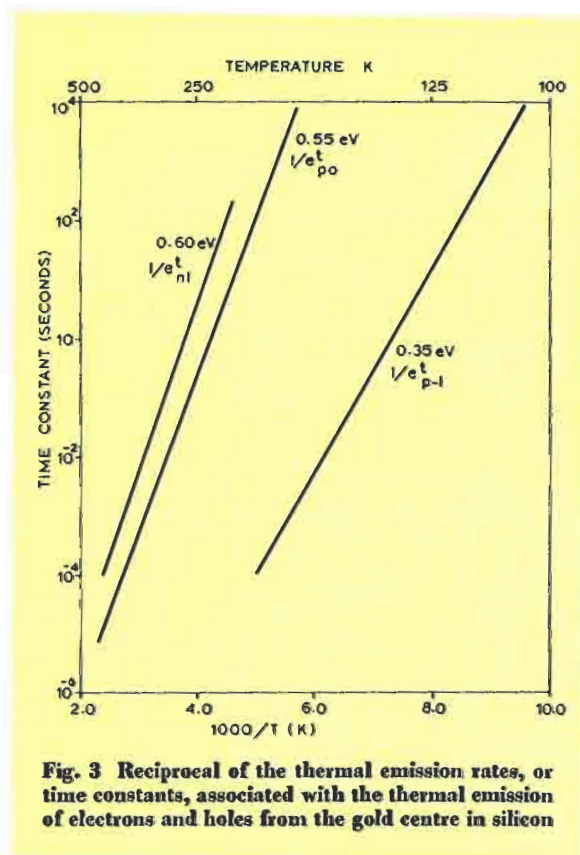


Fig. 3 Reciprocal of the thermal emission rates, or time constants, associated with the thermal emission of electrons and holes from the gold centre in silicon

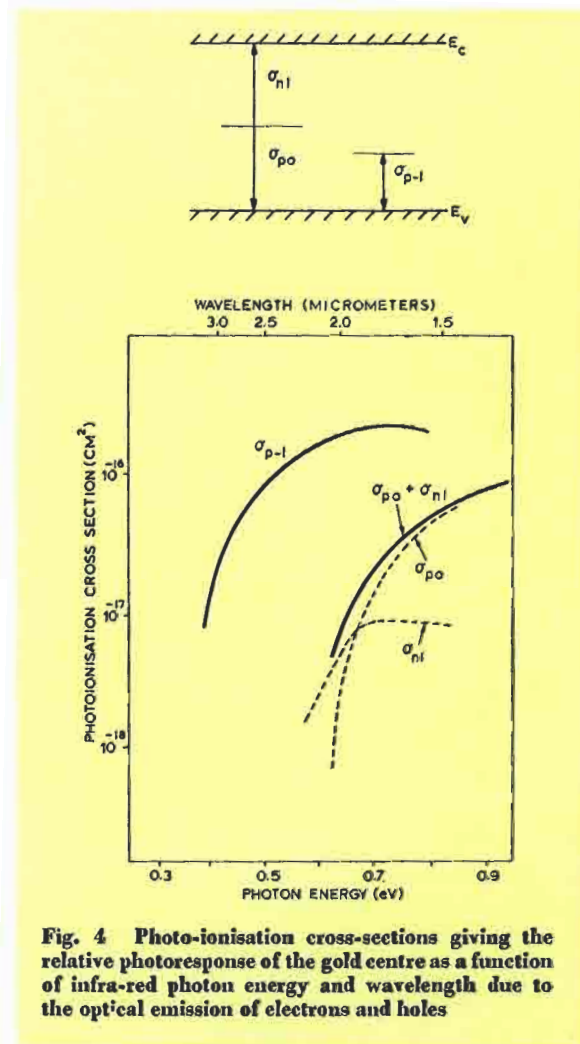


Fig. 4 Photo-ionisation cross-sections giving the relative photoresponse of the gold centre as a function of infra-red photon energy and wavelength due to the optical emission of electrons and holes

this process is known as optical emission or photo-ionisation. The optical emission rate, as for instance e_{p-l} , is proportional to the incident infra-red flux, Φ , and the photo-ionisation cross-section, σ_{p-l} . By illuminating either $p-n$ junctions or MOSFET device structures at low temperatures one can determine the photo-ionisation cross-sections as a function of the wavelength or photon energy of the infra-red radiation. This is shown in Figure 4. Again, since the acceptor level is near the centre of the band-gap, both hole and electron emission are important for this level. Conversely, this effect can be used to detect infra-red radiation by observing most conveniently the drain current of a MOSFET under infra-red illumination (6).

These techniques can also be modified to allow a determination of capture rates or capture coefficients by using visible light which is strongly absorbed by the silicon to generate carriers in the depletion region of the junction devices. If the temperature is low then again thermal emission will be eliminated and the capture of these carriers

can be observed. At low temperatures and at an average electric field of 4×10^4 Volts/cm this then yields values for the capture coefficients of $c_{no} = 1.7 \times 10^{-9}$ cm³/sec, $c_{pl} = 9.0 \times 10^{-8}$ cm³/sec, and $c_{po} = 5.5 \times 10^{-8}$ cm³/sec (4). These compare favourably with the values reported at room temperature and with no electric field by Fairfield & Gokhale (8) of 1.65×10^{-9} , 1.15×10^{-7} , and 2.4×10^{-8} cm³/sec respectively. They also give the value for c_{n-1} as 6.3×10^{-8} cm³/sec (8).

Infra-red Detector Applications

As shown in Figure 5, the gold-doped MOS transistor or MOSFET can be used as a very sensitive detector of infra-red radiation in the 1.0 to 3.0 micrometer wavelength regions (6). The change of gold impurity charge state in the surface depletion region of the MOSFET device structure due to optical emission or photo-ionisation causes a modulation in the conductivity between the drain and source of the transistor. The infra-red detector must be operated at low temperature, most conveniently at liquid nitrogen temperature of 77K, to eliminate thermal emission, and the charge state of the gold centre initially set to be in the most positive charge state.

The charge state of the gold impurity centre can be set initially by removing either the gate or backgate bias and allowing the surface depletion region to collapse, or this region to become occupied by a large concentration of holes from the substrate. When this large concentration of holes is present gold centres will capture holes and be left in the most positive charge state. Bias is now applied both to form the surface depletion region and to turn the transistor to the normal conducting state by the application of a positive gate voltage, V_{GS} . If infra-red radiation now illuminates the device, these gold centres can, in the simplest case, emit holes to the valence band and become less positive or neutral. Since the charge in the depletion region is becoming more negative it can do so only at the expense of negative charge in the channel of the MOSFET, or the number of electrons in the channel of the transistor must decrease and the conductivity of the transistor must decrease as shown in Figure 5.

The infra-red sensing MOSFET is an integrating detector, and the amount of the decrease in conductivity of the transistor is proportional to the total number of infra-red photons which have been incident on the detector since the beginning of the integration period. Responsivities of 500 Amp/Watt have been observed, or in other words, each incident photon results in a change in the current of 300 electrons and the device has a positive gain as the result of the transistor action (6).

It is proposed that this type of integrating infra-

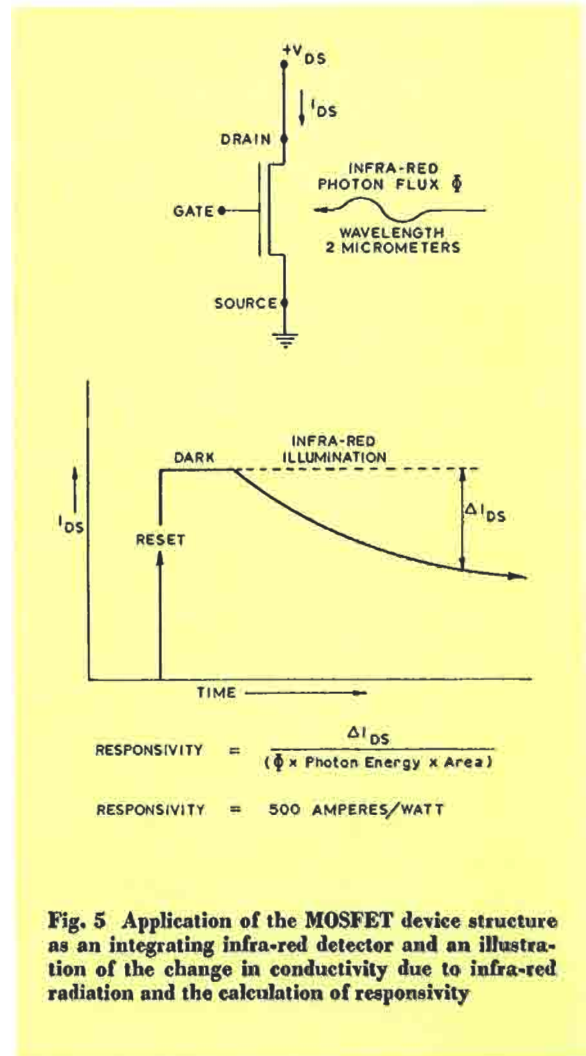


Fig. 5 Application of the MOSFET device structure as an integrating infra-red detector and an illustration of the change in conductivity due to infra-red radiation and the calculation of responsivity

red detector might be most useful in infra-red imaging. In the case of gold-doped devices this imaging would be near in the near infra-red wavelength region and could be employed for instance to locate and track the hot exhausts of aircraft or missiles which emit a large amount of radiation in the near infra-red.

Conclusions

The indirect observation of impurity centre charge states in the depletion regions of semi-conductor device structures cannot only be employed to provide an almost complete characterisation of these centres, but also can be employed to determine residual concentrations of impurities in semi-conductor devices and in the construction of very sensitive infra-red detectors. The specific example reviewed here has been the characteristics of gold in silicon and the application of gold-doped silicon devices as infra-red detectors. Similar techniques can, of course, be applied to all impurity centres in

silicon, although gold is perhaps one of the best known and widely used deep level impurity centres.

Acknowledgements

The author would like to acknowledge the invaluable contributions to the development of the concepts described here by his former thesis advisor at the University of Illinois, Professor C. T. Sah, and his continued interest and collaboration in work since that time. Some of the results summarised here have been taken from the author's Ph.D. thesis at the University of Illinois, work which was supported by the U.S. Air Force Office of Scientific Research and Defense Advanced Research Projects Agency. Other results have been summarised from work in conjunction with W. C. Parker at the University of Arkansas, the latter and this work at the University of California at Davis have also been supported by the Defense Advanced Research Projects Agency.

The Electroless Deposition of Gold

INFLUENCE OF THE SUBSTRATE STRUCTURE

Many types of electroless gold deposition processes have been proposed over the past fifteen years or so, but there is little doubt that the most successful solution was that devised in 1969 by Y. Okinaka at Bell Telephone Laboratories. This is based upon the use of an alkali metal borohydride, and it has found a number of applications in the fabrication of electronic components, although the process is still regarded as being complementary to, rather than competitive with, normal methods of electrodeposition, particularly where its catalytic characteristic is essential. Furthermore it has been the subject of intense investigation over the intervening years, both in respect of its mechanism of operation and of the structure and properties of the deposits (1).

The Okinaka bath is capable of producing sound if rather soft deposits of high purity gold, but the degree of porosity to be expected varies appreciably with their crystal structure, and this in turn depends largely upon the crystallographic orientation of the substrate as well as on the conditions of deposition.

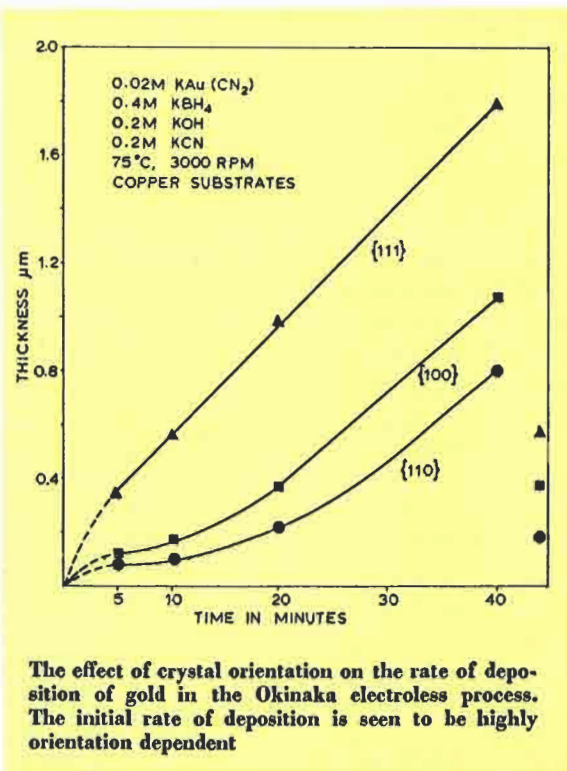
The most recent paper by two of Dr. Okinaka's colleagues, R. Sard and B. C. Wonsiewicz (2) shows that the orientation of the metal substrate may in fact have a profound effect on both the kinetics of the process and the structure of the deposits. The structure of gold deposits on single crystals of copper was studied at several stages of growth by means of a computer-aided X-ray pole figure technique, while additional data were secured by both transmission and scanning electron microscopy examination of the deposits. It was found that the initial rate of deposition could vary by an order of magnitude, the rate on {111} greatly exceeding that on {100}, which in turn gave a higher rate than on the {110} orientation.

In the early stages of deposition growth was epitaxial, but after a few minutes complex multiple twinning began to occur, and appeared to be responsible for a transition from the initially slow rate of deposition to the faster rate typical of the {111} orientation.

Deposition on polycrystalline substrates, including commercial copper strip, in both the cold rolled and the annealed conditions, was found to be in fairly

References

- 1 C. B. Collins, R. O. Carlson and C. J. Gallagher, *Phys. Rev.*, 1957, **105**, 1168
- 2 W. M. Bullis, *Solid-State Electron.*, 1957, **9**, 143
- 3 C. T. Sah, *Proc. IEEE*, 1967, **55**, 654
- 4 L. Forbes, 'Thermal and Optical Emission and Thermal Capture of Electrons and Holes at Gold Centers in Silicon,' Ph.D. Thesis, University of Illinois, Urbana, Illinois, U.S.A., 1970
- 5 C. T. Sah, L. Forbes, L. L. Rosier and A. F. Tasch, *Solid-State Electron.*, 1970, **13**, 759
- 6 W. C. Parker and L. Forbes, *IEEE Trans. on Electron Devices*, 1975, **ED-22**, 916
- 7 C. T. Sah, *Solid-State Electronics*, 1976, **19**, 975
- 8 J. M. Fairfield and B. V. Gokhale, *Solid-State Electron.*, 1965, **8**, 685
- 9 C. T. Sah, L. Forbes, L. L. Rosier, A. F. Tasch and A. B. Tole, *Appl. Phys. Lett.*, 1969, **15**, 145



general agreement with the results obtained on single crystals. The authors conclude that the substrate effects demonstrated in this work could be of equal importance in other catalytic methods of metal deposition and that this should prove to be a fruitful area for further research.

References

- 1 Y. Okinaka, in "Gold Plating Technology", ed. F. H. Reid and W. Goldie, Ayr, 1973, pp. 82-102; W. S. Rapson and T. Groenwald, *Gold Bull.*, 1975, **8**, (4), 119-126
- 2 R. Sard and B. C. Wonsiewicz, *J. Electrochem. Soc.*, 1976, **123**, (11), 1604-1612