High Speed Electro-optic Gating System Design Based on FPGA*

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Abstract: A novel approach called high speed electro-optic gating system was introduced to obtain the high speed electrical modulation signal. The system consists of two modules: gating pulse module and high voltage modulation module. The gating pulse module includes high-speed signal amplifier, FPGA (Filed Programmable Gate Array) delayer and controllable delayed transmission-line. The integration of the significant control function into FPGA achieves a number of desired properties such as high density, high integrated, erasable, filed programmable, and modulation-flexible. The overall delay was separated into digital delay and analog delay, which were finished by FPGA and controllable delayed transmission-line respectively. Experiments show that the system can generate a high-voltage rectangular electrical pulse with repetition frequency 1 Hz to 1 kHz, stepping 1 Hz, delay range from 0 to 1 μs, stepping 1ns, high voltage range from 0 V to 8 000 V, rising edge and falling edge within 10ns, jitter within 1ns. It can be applied to various electro-optic equipments.

Key words: Electro-optic modulation; *Q*-switched laser; FPGA(Filed Programmable Gate Array); Electro-optic gating system

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0 Introduction

Electro-optic effect is a physical phenomenon that the refractive index of some medium was changed under external electric field. The process of modulating beam by electro-optic effect is called electro-optic modulation. Since it is widely used in many areas such as optical communication[1], *Q*-switched laser[1], laser ranging, optical data storage[2], laser radar[3], laser holography, optical storage etc. The electro-optic modulation technology plays an important role in communication, precision manufacture and national defense. Acquisition of electrical modulation signal is a key component in electro-optic modulation. This article introduces a novel method to obtain the high speed electrical modulation signal. The system consists of two modules: gating pulse module and high voltage modulation module. The gating pulse module includes high-speed signal amplifier, FPGA delayer, controllable delayed transmission-line[4] and it can acquire external trigger signal and display its frequency, control the repetition frequency and delay generate low-voltage delay and real time monitor signal. High-voltage modulation module supplies high-voltage electrical pulse to Pockels cell. The significant control function of system could be integrated in FPGA with a number of desired properties such as high density, high integrated, erasable, filed programmable, and modulation-flexible. The overall delay was separated into digital delay with a length of integral times cycle of trigger signal at the FPGA and analog delay with a length of 0～16.5 ns at the controllable delayed transmission-line.

1 Design of high speed electro-optic gating system

1.1 Design principles

As shows in figure 1, electro-optic *Q*-switched indicates installing polarizer (P_1 and P_2) and KDP Pockels cell in laser resonator cavity to generate giant pulse. Beam is transformed to linearly polarized light via a linear polarizer. Under an electric field with $\lambda/4$ voltages, the phase of linearly polarized light changes $\Pi/2$ when it is transmitted via crystal since the beam can't travel through the resonator cavity in low value *Q* state (the phase of the linear polarized light would be otherwise unchanged without the electric field). As a result of this external effect, known as the Pockels effect, the quantity of top energy level

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particles increase rapidly. When the voltage on crystal is suddenly removed, the beam can transmit through the crystal freely and the resonator cavity is now in high value Q state, thereby creating giant laser pulses. The voltage supply scheme to Pockels cell is shown in the left bottom part of figure 1: S_1 and S_2 are equipments which amplify the gating pulses FD and FF generated by low-voltage module to high-voltage signal V_1 and V_2. Because V_2 owns a delay time TD relative to V_1, a high-voltage V_p[5] with a duration of TD is generated between two sides of the Pockels cell. It can control the value of Q which changes regularly to realize electro-optic modulation.

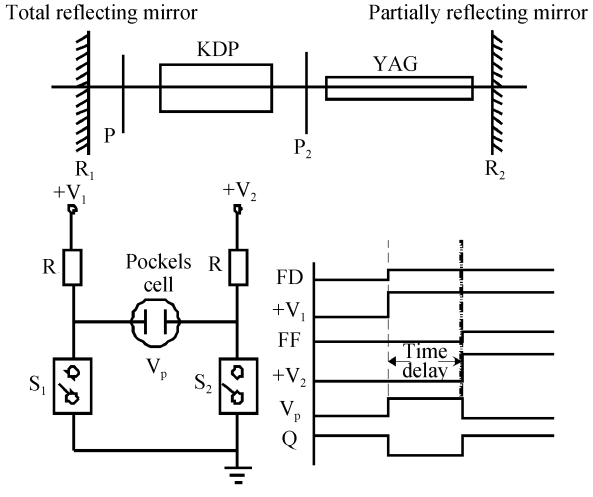

Fig. 1 Application of electro-optic gating system in Q-switched laser

Fig. 2 shows the control plane of electro-optic system. The frequency of zero-delay output V_1 and delay output V_2 is F_{cycle} with its modulation range from 1 Hz to 1 kHz, stepping 1 Hz. The delay of the rising edge from V_1 to V_2 is T_{delay} which ranges from 1ns to 0 to 1 μs, stepping 1 ns. The frequency of the external trigger signal (Trigger) is $F_{trigger}$ with a cycle of T_{base}. The system requires that FD and Trigger are synchronous. The monitor

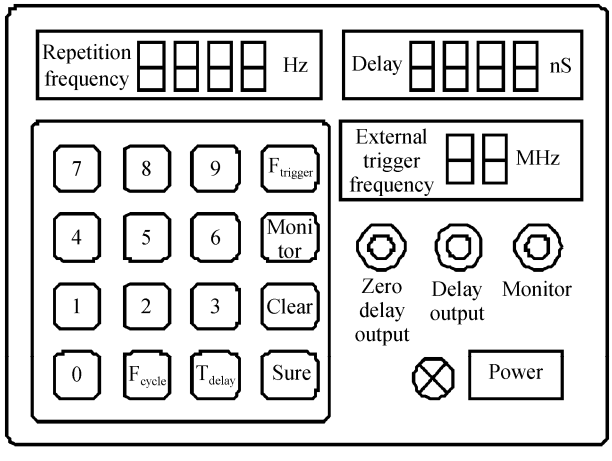

Fig. 2 Plane of the electro-optic gating system

which generates the similar wave as V_P displays the length and quality of the pulse V_P. Also, F_{cycle}, T_{delay} and $F_{trigger}$ can be set and displayed digitally by the panel.

1.2 Implementation of the electro-optic gating system

Since the time base of this system is the Trigger whose frequency is approximately 80MHz, it's impossible to realize a delay signal[6] which ranges from 1ns to 1 μs, stepping 1 ns in an absolutely digital way. A novel method of combining digital delay $T_{digital}$ and analog delay T_{analog} is used to realize this function in this article, as shown in equation(1). $T_{digital}$ can be achieved by a counter with mode n, explained in equation (2), using the Trigger as its clock, whereas T_{analog} comes from the controllable delayed transmission-lines. Both n and T_{analog} are calculated with Equation (3) and (4).

$$T_{dealy} = T_{digital} + T_{analog} \quad (1)$$

$$T_{digital} = nT_{base} \quad (2)$$

$$n = [T_{base} F_{trigger}/1000] \quad (3)$$

$$T_{analog} = T_d - 1000n/F_{trigger} \quad (4)$$

As shown in figure 3, signal FC and FCL are generated by PLL (phase locked loop) with its 20 MHz source clock from the crystal oscillator. FC shares the same frequency and rising edge to FCL but has a less duty. As FD and FDL gain from FC and FCL respectively through D flip-flops as Trigger for their clock, they are synchronous to external trigger signal Trigger. C_delay with a delay cycle of $T_{digital}$ is the delay signal generated from a controllable counter with FDL as enable signal, Trigger as clock, n as control mode. FM which is lagged with a time length $T_{digital}$ form FD can be generated from FD through a D flip-flop

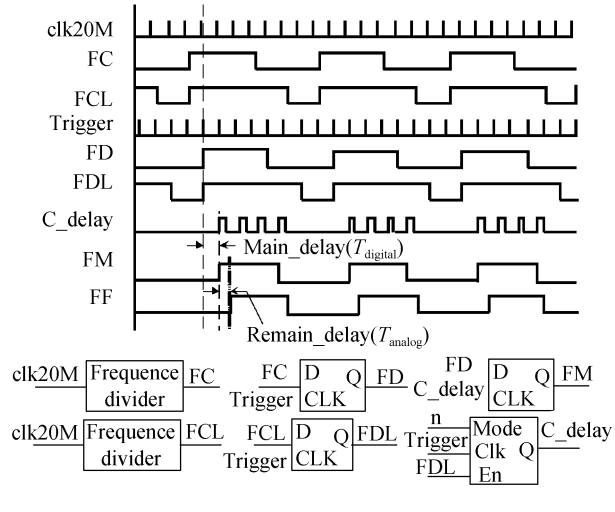

Fig. 3 Implementation of electro-optic gating system

with C _ delay as its clock. And FF can be generated from FM through transmission-line with analog delay T_{analog}.

1.3 Configuration of the gating system

The configuration of electro-optic gating system is shown in figure 4. Crystal oscillator is supplied with a 20MHz stable clock. It has two functions: one is for AS (Active Serial) configuration device as series input clock to write the configuration data to FPGA, and the other is for system as a source clock (clock _ source). Matrix keyboard receives the scan signal kb_in[3..0] from the FPGA and sends the feedback signal kb_out[3..0] to the FPGA. Thus, the inputs from keyboard by pressing the button can be recognized. JTAG (joint test action group) is a standard interface[7] in industry and is commonly used for testing and debugging. JTAG has the priority over any other configuration[8]. PIN (positive intrinsic negative) diode transforms the feedback signal of laser to external original time base signal with amplitude of approximately 200mV, which is then amplified to a CMOS (combinational metal-oxide semiconductor) logic level to match the FPGA. It is also used as external trigger signal Trigger. FPGA sends controlling codes to relays which control the connection of the transmission-lines. Thus, 1ns stepping delay is obtained. The display module controlled by FPGA can monitor the repetition frequency F_{cycle}, external trigger signal frequency $F_{trigger}$ and total delay T_{delay} conveniently.

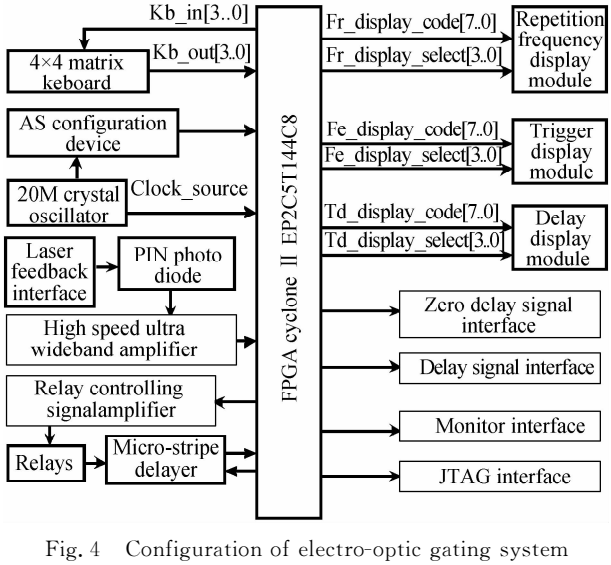

Fig. 4　Configuration of electro-optic gating system

1.4 Internal structure of FPGA

This system integrates main function to FPGA and implements data input, data process, display data output, digital delay, transmission-line controlling code generation. As shown in figure 5, crystal oscillator supplies a synchronous clock for sequential unit of the system and generates local clocks of 1 KHz and 10 KHz by a frequency divider. Matrix keyboard scan signal is generated by the 1 KHz clock. Display module is driven by the 10KHZ clock to display all the data at the same time. The keyboard de-jitter and encode module processes the combination of kb_in[3..0] and kb_out[3..0] to generate data sequence and command sequence. Divide number calculating unit produces the divide number by F_{cycle} then, the repetition frequency generating unit produces the signal FC and FCL by the divide number. As noted above, the rising edge of FC and FCL are synchronous and the duty of FCL is longer than FC. External frequency calculating unit and delay calculating unit product trigger frequency $F_{trigger}$ and delay time T_{delay} by the data input via keyboard. Digital delay cycle calculating unit products n with the command sequence according to Equation 1.3, then the digital delay unit completes a digital delay with a length of nT_{base} to generate FM from FD. Relay control signal unit generates relay controlling code to control the transmission to realize analog delay. The output of transmission line FF and repetition cycle signal FD generate monitor signal according to the logic circuit shown in figure 6. The state machine[9] generates the digital display signal and the controlling signal.

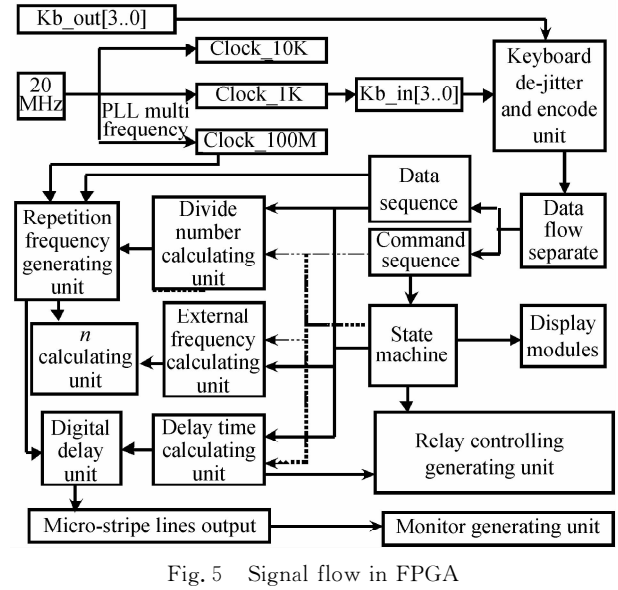

Fig. 5　Signal flow in FPGA

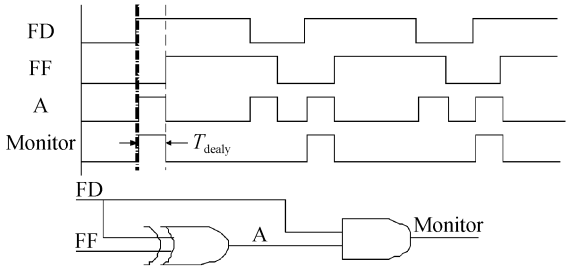

Fig. 6 Monitor signal generating circuit

2 Realization of analog delay

FPGA calculates analog delay time T_{analog} and the relay controlling code according to T_{delay} and $F_{trigger}$. The analog delay module consists of five double-pole double-throw relays and five snake-ship transmission line to realize delays of 8, 4, 5, 1, 0.5 ns as shown in figure 7. Delay transmission line is made up of micro-strip which was laid on glass-epoxy resin. The length of micro-strip can be calculated by Equation (6) according to the respective delay time. In order to satisfy the integrity constraint of the signal, 50Ω matching impedance is required[10]. Ignoring the thickness of the line, by measuring the thickness of the PCB (printed circuit board) h, its width w can be calculated according to Equation (5)[11]. Different combination of the five micro-strip line which is determined by relay controlling code can be used to realize 0 to 15.5 ns analog delay.

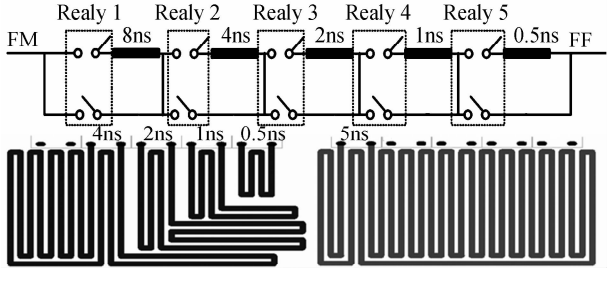

Fig. 7 Principle of analog delay

$$\text{Impedance}(\Omega):\frac{87}{\sqrt{\varepsilon_r+1.41}}\ln\left(\frac{5.98h}{0.8w+t}\right) \quad (5)$$

$$\text{propagation}(\text{ps/in}):85\sqrt{0.475\varepsilon_r+0.67} \quad (6)$$

3 High-voltage gating pulse generating module

Figure 8 shows a reliable method[12] of stacking power MOSFETs[13]. The resistor values are not critical and are used to set the dc operating voltages. Every power MOSFET can load hold off voltage of approximately 1 000 V. This system applies nine-level MOSFET stacking to amplify FD and FF to V_1 and V_2.

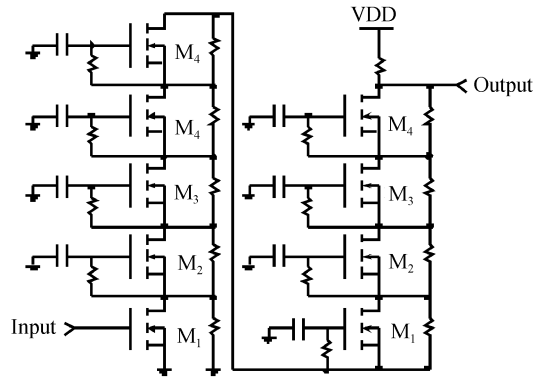

Fig. 8 Nine-level MOSFET stacking technology

4 Conclusion

After discussing the significance of modulation electrical pulse in electro-optic modulation, this article presents a high-speed electro-optic gating system based on FPGA. It introduces the principle of the generation of the modulation electrical pulse and separates the system to two modules: the gating pulse module and the high voltage modulation module, where the former one consists of high-speed signal amplifier, FPGA delayer and controllable delayed transmission-line. Experiment shows that the system can generate a high-voltage rectangular electrical pulse with repetition frequency 1 Hz to 1 kHz, stepping 1 Hz, delay range from 0 to 1 μs, stepping 1ns, high voltage range from 0 to 8 000 V, rising edge and falling edge within 10 ns, jitter within 1ns. It can be applied to various electro-optic equipments.

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基于 FPGA 的高速电光选通系统设计

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摘　要：介绍了一种获取高速调制电信号的新方法—基于 FPGA 的高速电光选通系统. 此系统分为选通脉冲和高压调控两个模块. 选通脉冲模块由高速信号放大、FPGA 延时、可控延迟传输线三个部分组成. 利用 FPGA 高密度、高可靠性、可反复擦写和可以现场编程、灵活调制的特点，将整个系统的主要控制部分集成在 FPGA 中，并将延时分为数字延时和模拟延时两部分. 然后利用 FPGA 实现数字延时，可控延时线实现模拟延时. 经试验检测，高压部分可以产生重复频率 1 Hz～1 kHz，步进 1 Hz，延时范围为 0～1 μs，步进为 1 ns，幅度为 8 000 V，前沿和后沿小于 10 ns，抖动小于 1 ns 的高压矩形电脉冲，从而满足各种电光调制系统中的需要.

关键词：电光调制；激光调 *Q*；现场可编程逻辑阵列(FPGA)；电光选通系统

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