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Pd 在 *p* 型单晶硅(100)表面自催化化学沉积

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摘要: 研究了 Pd 在氢终止的 *p* 型单晶硅(100)表面的自催化化学沉积(AED). 在室温下将刻蚀过的硅片浸入常规的 HF-$PdCl_2$-HCl 溶液制备了 Pd 膜. 将沉积了 Pd 的基底作为工作电极, 用循环伏安法(CV)、原子力显微镜(AFM)和 X 射线光电子能谱(XPS)研究了 Pd 膜的阳极溶出行为和形貌. 结果表明, Pd 的生长遵循 Volmer-Weber (VW)生长模式, Pd 膜给出了很好的支持.

关键词: 自催化化学沉积; 阳极溶出; Pd; 原子力显微镜; *p* 型单晶硅(100)
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Autocatalytic Electroless Deposition of Palladium onto *p*-Silicon (100)

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Abstract: The autocatalytic electroless deposition (AED) of palladium onto *p*-silicon (100) with hydrogen termination was studied. Pd films were prepared by immersing the hydrogen-terminated silicon wafers into conventional HF-$PdCl_2$-HCl solution at room temperature. The anodic stripping behaviors and morphologies of the Pd deposits were studied using cyclic voltammetry (CV), atomic force microscopy (AFM), and X-ray photoelectron spectroscopy (XPS). The results showed that the Pd growth was in Volmer-Weber (VW) mode and the Pd film had good adhesion.

Key Words: Autocatalytic electroless deposition; Anodic stripping; Palladium; Atomic force microscopy; *p*-Silicon (100)

Electroless deposition is a technique that has been widely used in a variety of applications of the electronic and semiconductor industries such as selective depositing on patterned substrates, making ohmic contacts, preparing electrodes, and ulta-large scale integration (ULSI) metallization[1–3]. This technology has three fundamentally different mechanisms: autocatalytic, substratecatalyzed, and galvanic displacement[4]. The process of autocatalytic electroless deposition (AED) for metallization uses a complex electrolyte composition to allow the reduced metal itself to serve as a catalyst for further reductive deposition.

To deposit the metals on a semiconductor surface, one of the key issues is the reliability of the catalytic surface. In the literature reports on preparation of the catalytic seed layer on silicon, one simple method is *via* the AED process, namely immersion plating from a HF solution spiked with noble metal ions, usually Pd^{2+}[5,6] and Ag^{+}[7,8]. This technique allows the formation of metal deposits in the form of island-like structure with simplicity in operation and lower cost. Therefore, it is important and necessary to investigate the growth process of AED.

Karmalkar and Banerjee[9] reported the AED of Pd on crystalline silicon using conventional HF-$PdCl_2$-HCl silicon activator solution, in which the SiO_2 etching and Pd deposition occurred simultaneously. Namely, the surface of Pd deposition was a SiO_2 layer (SiO_2/Si) and not a silicon surface with hydrogen-termination. The obtained Pd films were non-adherent as they reported. In this paper, we studied the growth process of Pd AED on the clean and hydrogen-terminated silicon surface.

Cyclic voltammetry (CV), used to study the anodic stripping behavior, could provide important information such as stripping potential, peak area, and stripping efficiency. In the electroless deposition method, the adhesion intensity between the deposited metal and the substrate surface is characterized by the oxidation (stripping) potential difference $\Delta E_{p\text{-}ox}$, which is the potential difference between the monolayer metal film stripping and the bulk

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metal stripping peaks. Accordingly, CV has been developed in evaluating the electroless deposition of silver on silicon by studying the anodic stripping behaviors of silver-silicon and silver-silver[10,11]. Here, this aim is to investigate the electroless Pd deposition and further find the adhesion intensity and stability of Pd films on silicon.

1 Experimental

1.1 Instrumentation

A P47-SPM-MDT atomic force microscope (AFM, Solver) with tapping mode and a CHI-660 electrochemical workstation (USA) were used. The chemical composition of the Pd film was investigated using XPS, which was conducted on a PHI-5702 electron spectrometer using a pass energy of 29.35 eV and a Mg K_α line as excitation source with the reference of C 1*s* at 284.6 eV. The resolution of the analyses for binding energy is 0.3 eV. The pressure in the analysis chamber was maintained at 6.5×10^{-7} Pa or lower during the measurements.

A homemade Teflon cell (40 mL) was used with a three-electrode configuration[12]. The silicon wafer was served as the working electrode with a disc area of 0.071 cm^2, which was mounted to a small hole of the bottom of the cell. The counter electrode was a platinum wire, dipping directly into the supporting electrolyte. The reference was saturated calomel electrode (SCE), connected to the electrolyte by means of a saturated KCl-agar salt bridge made of a Teflon tube.

1.2 Chemicals and materials

The stock solutions of 1.0 g·L^{-1} (0.01 mol·L^{-1}) $PdCl_2$ in 0.2 mol·L^{-1} HCl, 10% HF (volume fraction) in plastic bottle, and 0.5 mol·L^{-1} KCl as supporting electrolyte were used. All reagents are analytical-reagent grade. Milli-Q water (Millipore. 18.2 MΩ·cm^{-1}) was used throughout. A *p*-type Si (100) wafer with resistivity of 15–20 Ω·cm^{-1} and thickness of (650±25) μm (Beijing Youyan Silicon Villa Semiconductor) was used.

1.3 Wafer treatment

The silicon wafer was cut to produce square samples with 1 cm^2 surface area. Firstly the wafer was cleaned in an ultrasonic cleaner in absolute alcohol for 10 min. Then the wafer was immersed into a hot solution (80 ℃) of H_2O_2:NH_4OH:H_2O (1:1:5, volume ratio) for 10 min and next into another hot solution (80 ℃) of H_2O_2:HCl:H_2O (1:1:6 volume ratio) for 10 min to remove possible contamination. Finally the wafer was etched in a solution of 10 mL HF (40%)+100 mL NH_4F (40 g NH_4F in 100 mL H_2O) for 2 min at room temperature, to prepare a clean and hydrogen-terminated surface. The wafer was rinsed with water and dried with nitrogen flux after each cleaning step.

1.4 AED process

The Pd AED process was carried out by immersing the etched silicon wafer into a solution of 0.005 mol·L^{-1} $PdCl_2$+0.1 mol·L^{-1} HCl+0.4% (0.24 mol·L^{-1}) HF for different time at room temperature, and then rinsed with water and dried with dry nitrogen flux.

1.5 CV procedure

After deposition, the substrate was mounted to the cell. As the electrolyte solution of 0.5 mol·L^{-1} KCl was added and it was ensured that there were no bubbles on the surface of the wafer, CV scanning was immediately performed. The potentials were initially scanned in the positive direction from −0.5 V, and the oxidation peak was taken as positive current.

2 Results and discussion

2.1 Characterization of electrolessly deposited Pd film

The three-dimensional (3D) atomic force microscopy (AFM) image (2 μm×2 μm) of the blank *p*-type silicon (100) wafer is shown in Fig.1. It can be seen that the blank wafer itself is flat enough so the signal is almost at noise level. The etching method has been shown to create a hydrogen-terminated silicon substrate surface with hydrogens bonded to the surface and with a defect density of about 0.5% [13].

Fig.2 presents a set of 3D AFM images (3 μm×3 μm) of the Pd films deposited for 1 s, 5 s, and 30 s. It is observed that the substrate was covered with a palladium thin film in the form of islands. In comparison with Fig.1, Fig.2a shows more clearly the image of palladium nuclei, while in Fig.2(b, c), larger and thicker grains were clustered around the nuclei. The results

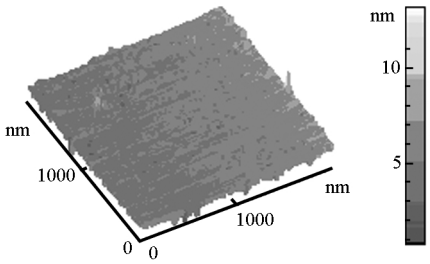

Fig.1 AFM image of the etched silicon

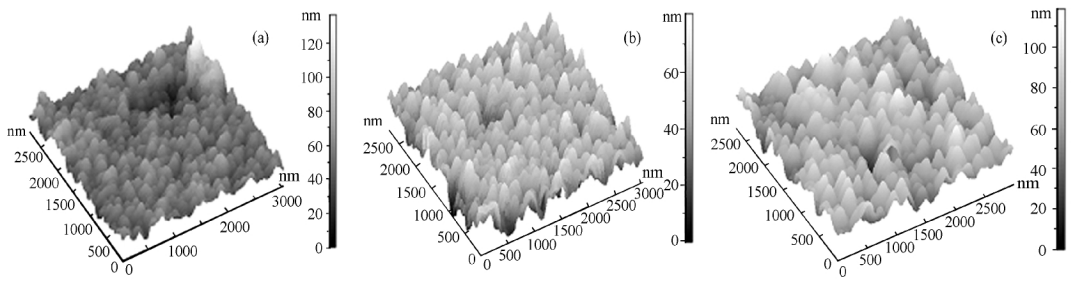

Fig.2 AFM images of the Pd films prepared by immersing the etched silicon into the solution of 0.005 mol·L^{-1} $PdCl_2$+0.1 mol·L^{-1} HCl+0.24 mol·L^{-1} HF for 1 s (a), 5 s (b), and 30 s (c)

showed that the initial deposition kinetics could be described by Volmer-Weber (VW) mode, i.e., the growth process includes: nucleation of palladium started on surface defects which were thermodynamically favorable for deposition[14]; and once a stable Pd nucleus was formed, it acted as a cathode; thus, palladium ions were continually reduced to neutral atoms, which were clustered around the nuclei. Furthermore, it was observed that no Pd deposits peeled off, indicating the obtained film had good adhesion strength. However, the discontinuous growth was observed, i.e., larger grains were surrounded by smaller particles. This was because the growth of nuclei on the substrate and the displacement reaction were unbalanced.

The XPS spectrum of the electrolessly deposited Pd film is shown in Fig.3. Two Pd energy peaks assigned to the $3d_{5/2}$ and $3d_{3/2}$ energy level are located at 335.4 and 340.8 eV, respectively. The other two Pd peaks corresponding to the Pd $3p_{1/2}$ and $3p_{3/2}$ energy level are located at 560.4 and 532.8 eV. The weak Si 2*s* and 2*p* peaks can be observed at 99.6 and 150.8 eV, respectively. The spectrum confirms that the deposited film consists of Pd particles.

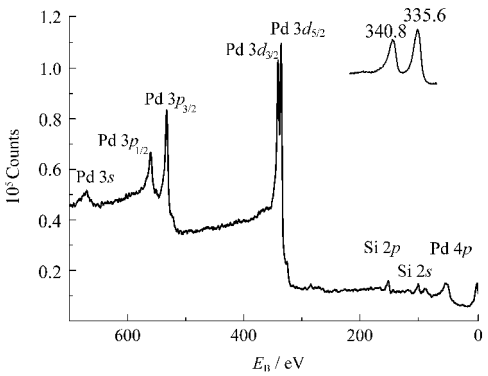

Fig.3 XPS spectrum of electrolessly deposited Pd film

The inset XPS spectrum is Pd 3*d*.

2.2 Anodic stripping behavior

For the stripping process of palladium deposited on silicon with CV, the electrode reactions can be expressed as the following:

$$Si\text{-}Pd - 2e + 4Cl^- \rightarrow Si\text{-}PdCl_4^{2-} \quad \text{MD-S} \quad (1)$$

$$Pd\text{-}Pd - 2e + 4Cl^- \rightarrow Pd\text{-}PdCl_4^{2-} \quad \text{BD-S} \quad (2)$$

Here, the Pd monolayer stripping (MD-S) potential is assigned to the peak located at a relatively positive potential, caused by the oxidation of the Pd-Si structure, while the bulk stripping (BD-S) potential is located at a relatively negative potential from the oxidation of the Pd-Pd structure.

Fig.4 shows the CV curves of the Pd layers on the silicon wafer for different deposition times. Compared with the CV curves for 5 s and longer deposition, the peaks of BD-S corresponding to 1 to 3 s deposition were not observed in Fig.4A. It is found that the potentials of MD-S peaks are primarily identical, about 2.7 V, and the current of the MD-S peaks increases with the increase of deposition time (*t*). In a word, the nucleation of Pd was dominant within 3 s.

With 5 s and longer deposition, the BS peaks locate at about 1.0 V and the peak current increase, with the increase of deposition time, while the potentials of MD-S peaks also stood at about 2.7 V and their peak current kept in the same order in value on the whole, which proved that the Pd AED was a VW growth process according to the definitions of MD-S and BD-S. The potential difference ($\Delta E_{p\text{-}OX}$) between MD-S and BD-S peaks was up to 1.7 V and increased slightly with the increase of deposition time *t*, which indicated that the Pd film obtained was with good adhesion strength. As mentioned above[9], Pd AED on the silicon surface with native silicon oxide was non-adherent. The cause might result from the different growth modes. Since the surface with native silicon oxide had no defects, and the Pd deposition and SiO_2 etching occured simultaneously, the adhesion of Pd and silicon surface was very weak. We assumed that its growth was only a galvanic displacement process. Contrarily, the defects of the hydrogen-terminated silicon surface were activated sites and Pd particles nucleated on the defects; then Pd film grew around the Pd nuclei. Its growth was typically a VW growth process. Therefore, the Pd film had fine adherent.

It should be pointed out that there exists another apparent peak near the MD-S peak. Some [15] supposed that the peak was created due to two steps of the electron transfer during Pd oxidation. However, we think that the supposition is not suitable to this system. One simple reason is the following: if the MD-S peak had two split peaks, the BD-S peak should be also split into two peaks, while we only observed three peaks rather than four peaks. We found that the stripping behavior of Pb was similar to that of Pd[16], and then proposed an analogous explanation: the peak nearby the MD-S peak may arise from Pd deposits at surface sites different from those at which the more stable monolay-

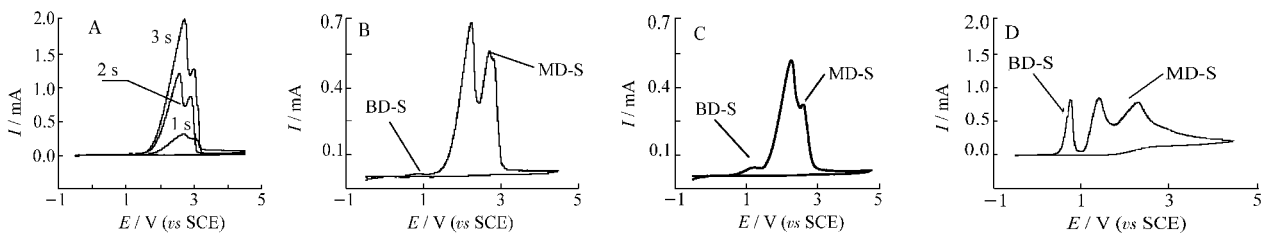

Fig.4 Cyclic voltammograms of Pd deposits on silicon for different times

A) The overlapped CV curves of 1 s, 2 s, and 3 s; B), C), and D) are the figures of 5 s, 10 s, and 60 s deposition, respectively. Supporting electrolyte is 0.5 mol·L^{-1} KCl solution. Scan rate is 50 mV·s^{-1}.

er is formed. Szabo[17] has noted the energetic heterogeneity of substrate surfaces and thus the existence of multiple energy states for monolayers. Alternatively, the peak may arise from stripping of the Pd layer next to that in direct contact with the silicon substrate. The atomic environment in this layer will be unique and the atoms will be partially stabilized by interaction with the electrode material.

3 Conclusions

In this paper, CV was used to investigate the AED process of Pd on *p*-Si(100) with hydrogen termination by studying the anodic stripping behaviors. The morphologies of the obtained Pd films were characterized with AFM and XPS. The experimental results showed that the Pd growth on hydrogen-terminated silicon wafers was a typical AED growth process, and the films had good adhesion strength.

References

1 Dubin, V. M.; Shacham-Diamand, Y.; Zhao, B.; Vasuder, P. K.; Ting, H. *J. Electrochem. Soc.,* **1997, 144**: 898

2 Dryfe, R. A. W.; Simm, A. O.; Kralj, B. *J. Am. Chem. Soc.,* **2003, 125**: 13014

3 Liu, J. B.; Dong, W.; Zhan, P.; Wang, S. Z.; Zhang, J. H.; Wang, Z. L. *Langmuir,* **2005, 21**: 1683

4 Poter, Jr. L. A.; Choi, H. C.; Ribbe, A. E.; Buriak, J. M. *Nano Lett.,* **2002, 2**: 1067

5 Inberg, A.; Zhu, L.; Hirschberg, G.; Gladkikh, A.; Croitoru, N.; Shacham-Diamand, Y.; Gileadi, E. *J. Electrochem. Soc.,* **2001, 148**: C784

6 Shacham-Diamand, Y.; Inberg, A.; Sverdlov, Y.; Croitoru, N. *J. Electrochem. Soc.,* **2000, 147**: 3345

7 Tong, H.; Zhu, L.; Li, M.; Wang, C. *Electrochim. Acta,* **2003, 48**: 2473

8 Jing, F.; Tong, H.; Kong, L.; Wang, C. *Appl. Phys. A,* **2005, 80**: 597

9 Karmalkar, S.; Banerjee, J. *J. Electrochem. Soc.,* **1999, 146**: C580

10 Jing, F.; Tong, H.; Wang, C. *J. Solid State Electrochem.,* **2004, 8**: 877

11 Ye, W.; Tong, H.; Wang, C. *Microchim. Acta,* **2005, 152**: 85

12 Tong, H.; Wang, C. M. *Acta Chim. Sin.,* **2002, 60**: 1923 [佟 浩, 王春明. 化学学报, **2002, 60**: 1923]

13 Higashi, G. S.; Chabal, Y. J.; Trucks, G. W.; Raghavachari, K. *Appl. Phys. Lett.,* **1990, 56**: 656

14 Choi, J.; Chen, Z.; Singh, R. K. *J. Electrochem. Soc.,* **2003, 150**: C563

15 Sun, Q.; Wang, C.; Li, L.; Li, H. *Fresenius J. Anal. Chem.,* **1999, 363**: 114

16 Matousek, J. P.; Powell, H. K. J. *Talanta,* **1997, 44**: 1183

17 Szabo, S. *Int. Rev. Phys. Chem.,* **1991, 10**: 207