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NEW HIGH-SPEED A-SI/C-SI- AND A-SIC/C-SI-BASED SWITCHES

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The electrical and optical characteristics of the new high-speed Al/a-Si/c-Si(p)/c-Si(n^+)/Al and Al/a-SiC/c-Si(p)/c-Si(n^+)/Al optically controlled switches are presented in this paper. These switches exhibit the lowest ever reported values of rise and fall times, for this kind of switches, of about 3ns. They also exhibit a temperature and light reversibly controlled forward breakover voltage (V_{BF}), together with high values of light triggering sensitivity.

INTRODUCTION

Heterojunctions between c-Si substrates and a-Si and its alloys have found applications in devices such as heterojunction bipolar transistors (HBT) [1–5] and metal-amorphous silicon FET's (MASFET) [6]. Novel device applications of the above heterojunctions are in the threshold switches, which use a multilayer structure of hydrogenated amorphous silicon thin films [7,8,9], and also in the memory switches using non-hydrogenated a-Si films [10]. Most of these switches exhibit low values (< 50V) of switching voltages [7,8,9,10], together with switching times in the range of microseconds. We present here, for the first time, the electrical and optical characteristics of high-speed heterojunction thyristor-like switches, which exhibit high values of forward breakover voltages (56-160V), with switching times in the range of nanoseconds, and which use only one layer of non-hydrogenated a-Si or a-SiC thin films.

EXPERIMENTAL

The switches were fabricated using three different types of c-Si(p)/c-Si(n^+) substrates. Type 1 substrates had a resistivity of 9 Ω-cm and 8×10^{-3} Ω-cm for the p-type and n^+-type regions, respectively, and a thickness of about 15.5 μm for the p-type region. Type 2 substrates had a p-type region thickness of about 23.5 μm, and the resistivities were 22 Ω-cm and 2×10^{-2} Ω-cm for the p-type and n^+-type regions, respectively. Type 3 substrates differed from type 2 substrates in that their c-Si(p) region was ion implanted with B^+ ions of energy 30 keV, at a dose of 9×10^{13} cm^{-2}, and was subsequently annealed at 860°C for 30 minutes in order to form a p^+-type thin layer of about 0.2 μm, with a peak carrier concentration of about 10^{19}

TABLE 1
A list of all types of samples fabricated in this work

Type 1 samples	Al/a-SiC/p/n^+(type-1 substrates)/Al
Type 2 samples	Al/a-SiC/p/n^+/(type-2 substrates)/Al
Type 3 samples	Al/a-Si/p/n^+/(type-1 substrates)/Al
Type 4 samples	Al/a-Si/p/n^+/(type-2 substrates)/Al
Type 5 samples	Al/a-SiC/p/n^+/(type-3 substrates)/Al

cm^{-3}. The a-Si or a-SiC thin films, of about 1 μm thickness, were deposited onto the c-Si(p) regions for all samples using the R.F. sputtering technique. We have described elsewhere [11,12] the R.F. sputtering conditions during deposition. Aluminum was used for the metalization of all samples. Table 1 shows a list of all types of samples fabricated in this work, and Figure 1 shows a cross-sectional view of the device.

The I-V measurements, at different temperatures, were performed on all samples under vacuum pressure of about 10^{-2} mbar in order to obtain temperature stability, especially for the low temperature region. The I-V characteristics were obtained by means of a curve tracer. The samples were connected in series with an 8kΩ resistance for protection upon switching. The light triggering sensitivity ($\Delta V_{BF}/\Delta P_i$) measurements were done using a monochromator for providing light of different wavelengths. The samples were connected to the curve tracer in order to obtain ΔV_{BF} values between dark and illumination conditions. In this measurement, P_i is the light power falling normal to the sample surface. Finally, rise and fall times of the switches were measured at a pulse frequency of 100MHz using a pulse generator connected in series with the samples, and an oscilloscope across a load resistance of 1kΩ connected in series with the samples. The DC power supply output was held at voltage values just below the forward breakover voltage (V_{BF}) for all samples during this measurement, and an additional positive square pulse of 5V was applied on the device in order to obtain the OFF-ON-OFF transitions.

RESULTS AND DISCUSSION

Typical I-V characteristics of type 3 and type 5 samples under dark and illumination conditions are presented in Figures 2 and 3, respectively. The I-V characteristics for

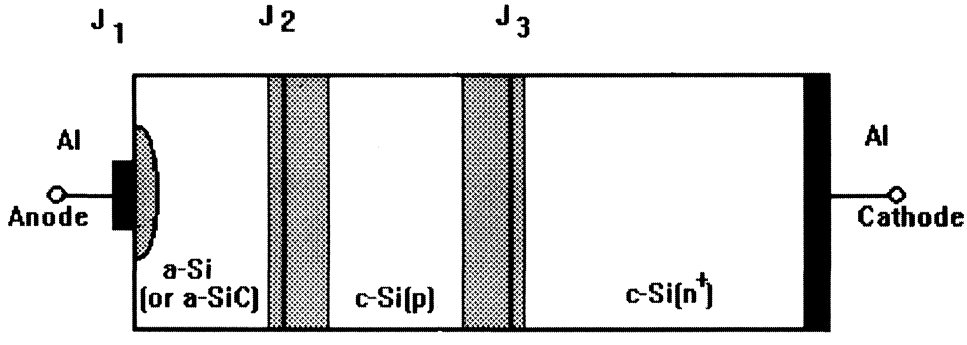

FIGURE 1 A cross sectional view of the Al/a-Si(or a-SiC)/c-Si(p)/c-Si(n^+)/Al devices.

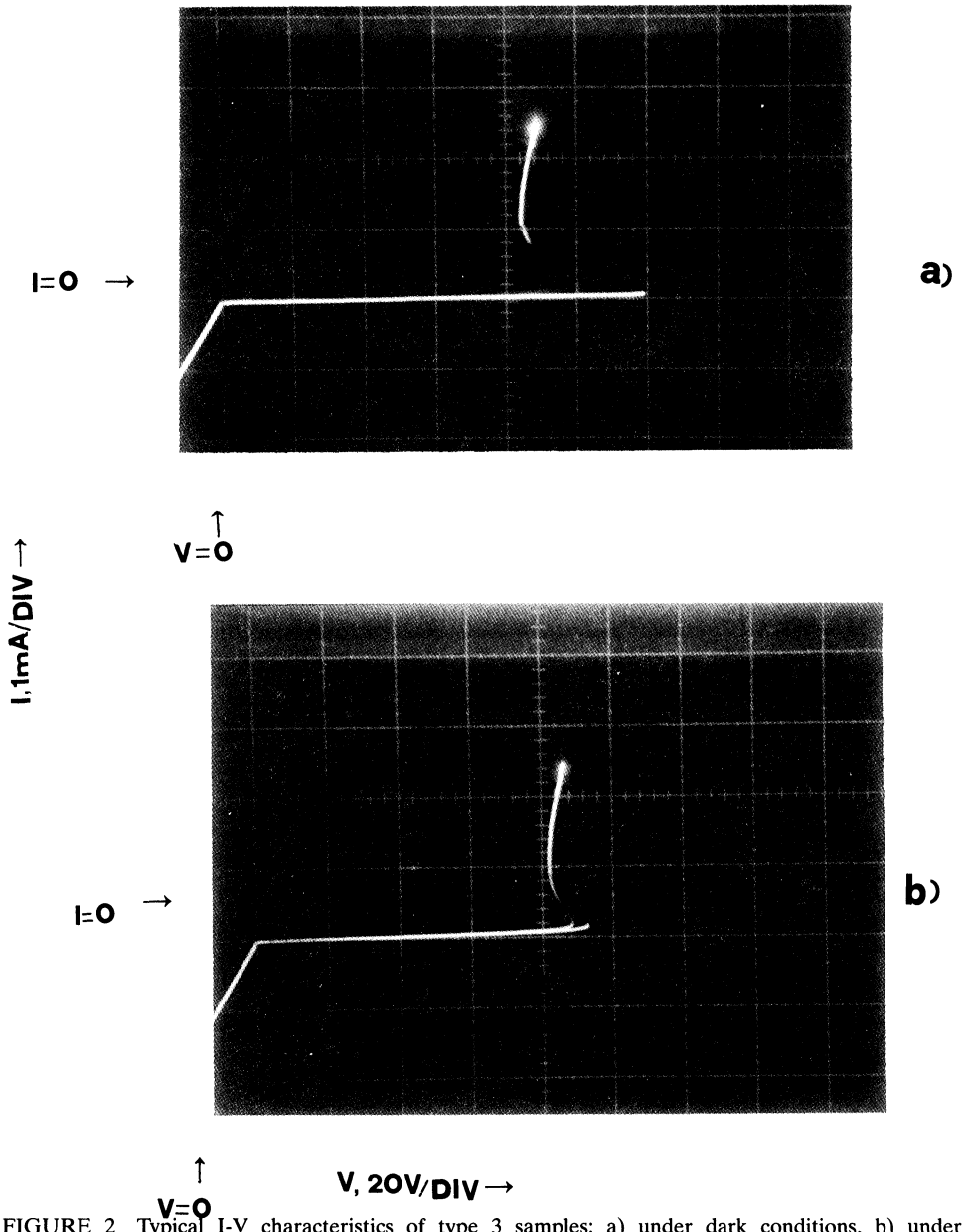

FIGURE 2 Typical I-V characteristics of type 3 samples: a) under dark conditions, b) under illumination conditions (light intensity ≈ 7 mW/cm^2).

type 1, 2, 3, and 4 samples were presented elsewhere [12]. It can be seen from the above figures that the behavior of the switches resembles that of a thyristor. The switches include three junctions, apart from the Al/c-Si(n^+) back ohmic contact. The junction Al/a-Si(or a-SiC) is junction 1 (J_1), the a-Si(or a-SiC)/c-Si(p) is (J_2), and c-Si(p)/c-Si(n^+) is (J_3) (Fig. 1). The devices are in forward bias conditions when a positive potential is applied to the Al layer of J_1 and a negative one to the

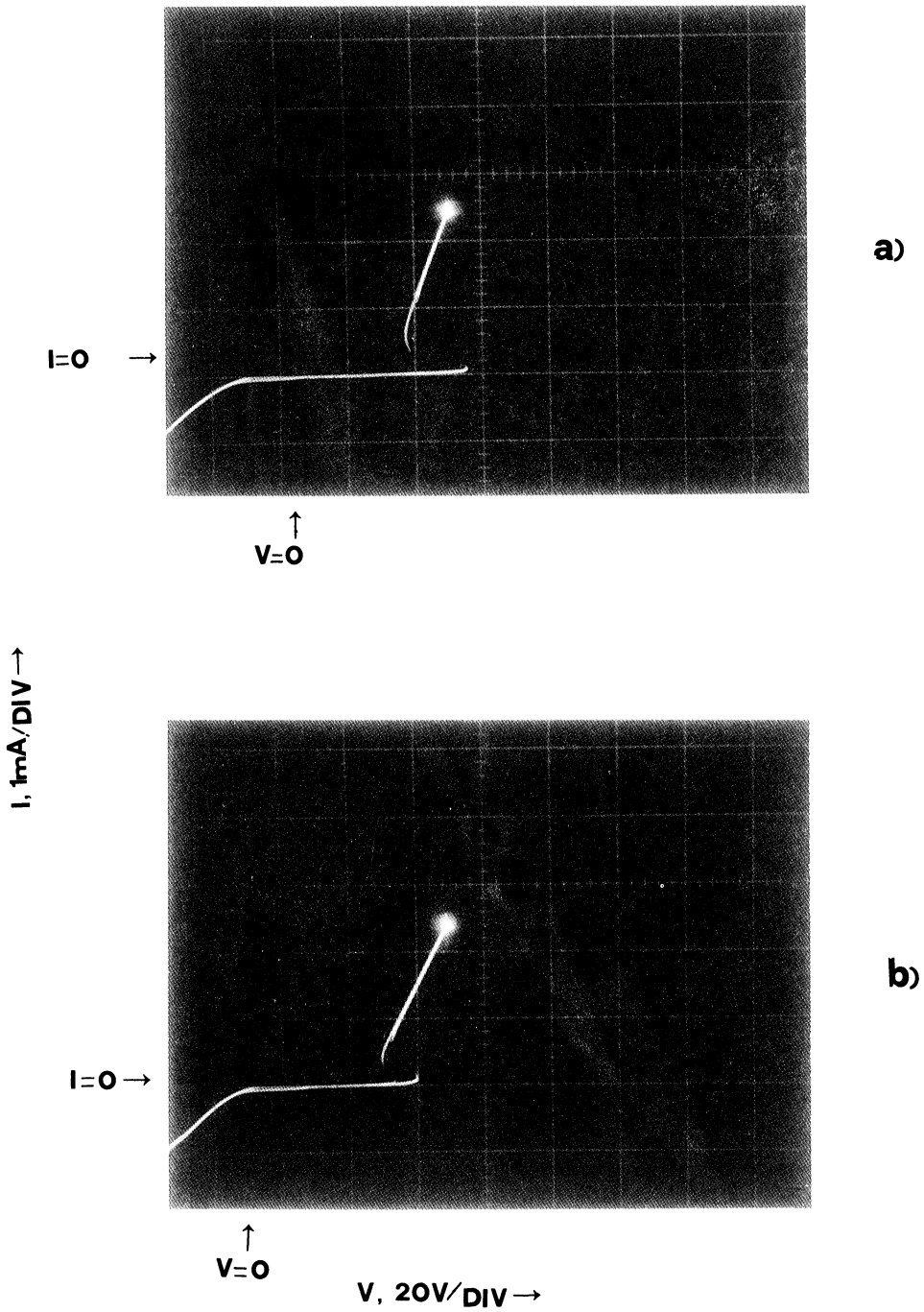

FIGURE 3 Typical I-V characteristics of type 5 samples: a) under dark conditions, b) under illumination conditions (light intensity $\approx$ 5.1 mW/cm^2).

back ohmic contact, which lead to forward bias conditions for J_1 and J_3 while J_2 is reverse biased, the main voltage drop occurs across this junction.

When the applied forward bias voltage across the device (V_{AK}) is low ($V_{AK} << V_{BF}$), the injected electrons from the c-Si(n^+) electron emitter, upon reaching the depletion region of the reverse biased junction J_2, decay via trapping and recombination, mostly in the amorphous part of J_2 depletion region. The trapping and recombination mechanisms also dominate in the forward biased junction J_1, thus preventing a hole flow from the p^+ hole emitter (Al) towards J_2. It is known [13] that the recombination current density in a forward-biased p-n junction is given by the relation:

$$J_{rg} \propto d/\tau_0 \exp(qV/2kT) \tag{1}$$

where d is the depletion region width, V is the bias voltage applied to the junction and τ_0 is the effective carrier lifetime in the depletion region. This lifetime is known to be affected [14] by the density of trapping centers (N_T) existing in the energy gap of the semiconductor, which in this particular case is the a-Si or a-SiC film with $N_T > 10^{17}$ cm^{-3} [15,16] as follows:

$$\tau_0 \propto 1/N_T \tag{2}$$

The carrier thermal generation rate in the depletion region of the reverse biased junction J_2 is small and the carrier multiplication factor is $M < 2$, as it may be found for $V_{AK} = V_2 < 80V$, using the relation:

$$M = \frac{1}{1 - \left(\frac{V_2}{V_B}\right)^n} = \frac{1}{1 - \left(\frac{E_2}{E_B}\right)^n} \tag{3}$$

where V_2 and E_2 are the voltage drop across J_2 and the electric field in J_2 depletion region, respectively, while V_B and E_B are the breakdown voltage and breakdown field of J_2, respectively, and $n = 4$ [14].

For values of $V_{AK} = V_{BF}$, the carrier multiplication factor $M \rightarrow \infty$ (eq. 3) and J_2 are in avalanche breakdown conditions. This is concluded from the fact that the breakdown voltage (V_B) for the Al/a-Si/c-Si(p)/Au and Al/a-SiC/c-Si(p)/Au heterojunctions, which were also fabricated during this work, was found to be $V_B \approx V_{BF}$, the forward breakover voltage of the switches based on either of the above heterojunctions.

As soon as J_2 falls into avalanche breakdown conditions, the excess of electrons generated within the depletion region causes the filling of traps in the amorphous depletion regions of J_2 and J_1, resulting in increased values for the effective carrier lifetime τ_0 and, finally, in a decreased recombination current density in the depletion region of J_1 (eqs. 1,2). The hole injection from the p^+-emitter (Al) and the electron injection from the n^+-emitter now dominate. This increases the

common base current gains α_1 and α_2 of the p^+-n-p and n-p-n^+ transistors, respectively, causing the known [14] from thyristor theory condition $\alpha_1 + \alpha_2 \approx 1$ to be reached, and as a result, the device falls into its conducting low-resistance (ON) state, as we have described elsewhere [12].

The strong carrier injection from both emitters in the ON state suggests that J_2 does not now need to maintain the avalanche breakdown conditions for supplying a large amount of generated carriers to the switch. The large values of forward voltage drop (V_F) in the ON state of the device, observed in Figs. 2 and 3 (V_F = 83V for type 3 samples, and V_F = 39V for type 5 samples), may be attributed to a specific current flow through the device, which has to be maintained in order to hold the device in the ON state by keeping the traps in the amorphous film filled. The above current flow is the result of a small-carrier thermal-generation rate in the depletion region of J_2 in conjunction with a strong injection of holes from the p^+-emitter and electrons from the n^+-emitter.

It should be mentioned here that all samples exhibit a reversible decrease of the forward breakover voltage (V_{BF}) with increasing illumination intensity (Figs 2 and 3). Increasing light intensity causes an enhanced carrier generation rate, especially within the depletion region of the reverse biased junction J_2. The applied forward bias across the device does not need to reach V_{BF} values in order to lead junction J_2 into avalanche breakdown conditions (for providing the excess carriers required for the transition into the ON state), because the light intensity generates the excess carriers needed. This results in the ON state transition at lower forward bias voltages.

In Figure 4 a, b, and c are shown the diagrams of V_{BF}(Volts) versus T(K), V_F(Volts) versus T(K), and I_h(mA) versus T(K), respectively, where V_F is the forward voltage drop across the switch in the conducting (ON) state, and I_h is the holding current (similar to that in a thyristor).

It can be seen from Fig. 4a that all samples exhibit a decrease in V_{BF} with increasing temperature. This decrease is more abrupt, for most of the samples, in the temperature range 280K–330K. These results are in qualitative agreement with other published data concerning a-Si:H [8], as well as c-Si switches [13,17]. We attribute this behavior to the variation of carrier thermal-generation rate with temperature. Increasing temperature above 300K causes an enhanced carrier generation rate in J_2, in a way similar to the increase of light intensity, resulting (as mentioned above) in the ON state transition at lower forward breakover voltages (V_{BF}). A typical I–V characteristic of type 3 samples, in the dark, for a sample temperature T = 322.8K is presented in Fig. 5a. When the temperature decreases below 300K, increased values of the applied voltage across the device (V_{AK}) are needed to compensate the reduced carrier thermal-generation rate, resulting in higher values of V_{BF}, as it may also be observed in the typical dark I–V characteristic of type 3 samples for a sample temperature T = 250 K presented in Fig. 5b.

In Fig. 4b, an increase in the forward voltage drop (V_F) with decreasing temperature is observed. We attribute this behavior to the reduction in carrier thermal generation rate caused by the decreasing temperature. Thus, the forward

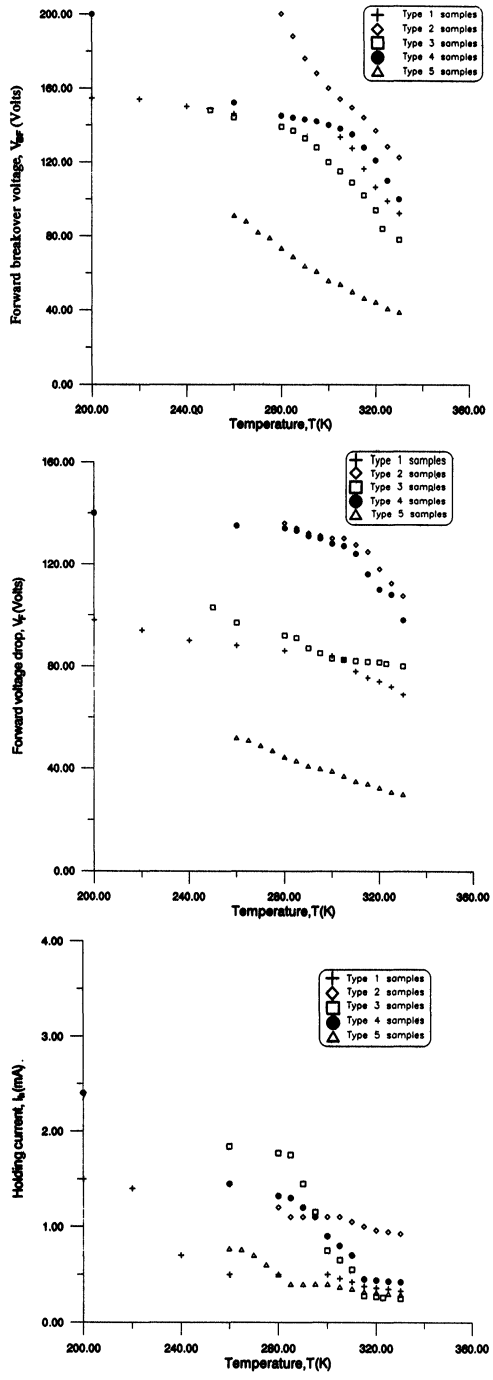

FIGURE 4 Temperature dependence of the: a) forward breakover voltage (V_{BF}), b) forward voltage drop (V_F) and c) holding current (I_h).

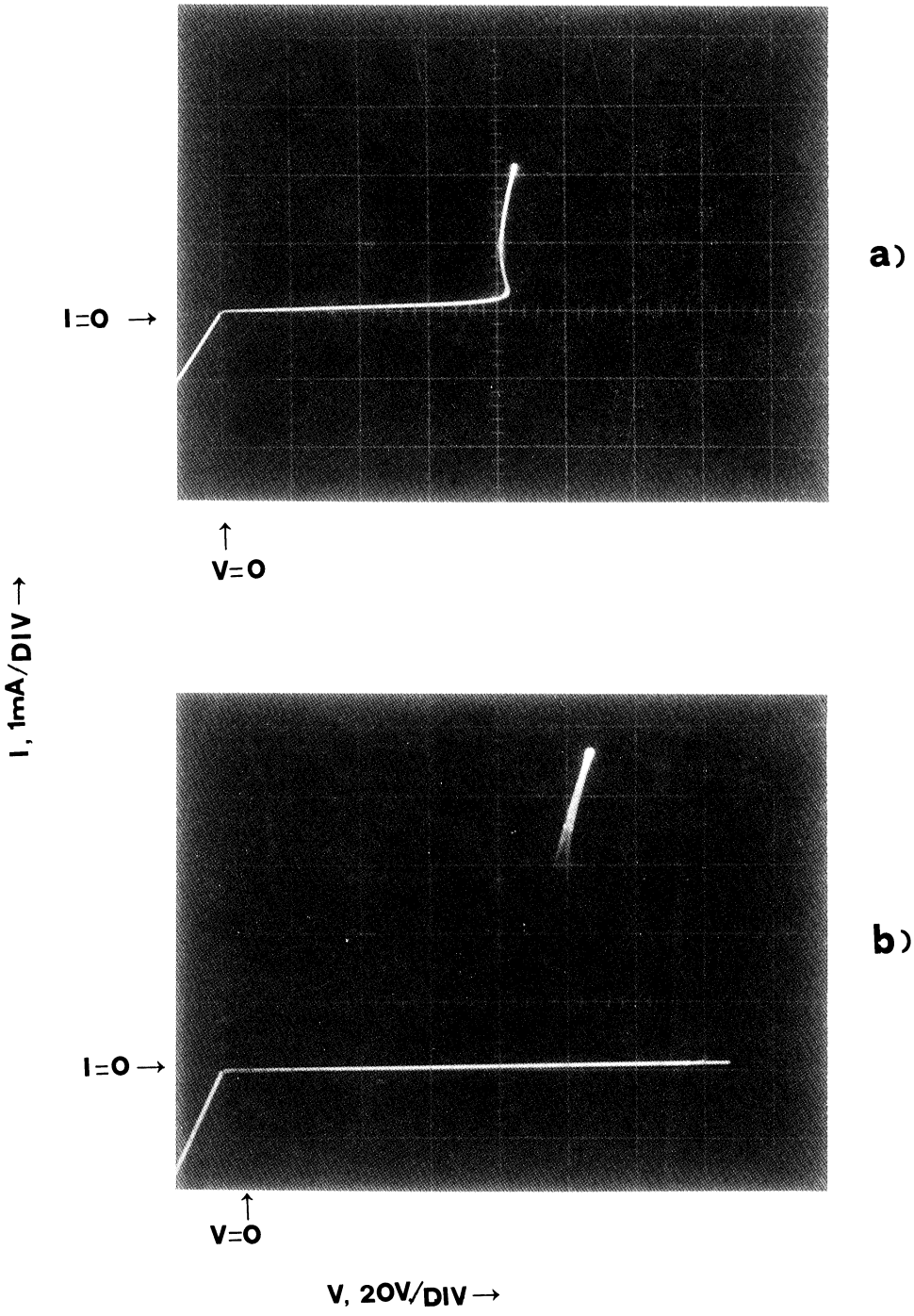

FIGURE 5 Typical I-V characteristics of type 3 samples, under dark conditions, for a sample temperature: a) T = 322.8 K and b) T = 250 K.

voltage drop (V_F) takes on higher values for the injection currents to compensate the reduced carrier thermal-generation rate and provide the current flow required for maintaining the ON state, as it was mentioned earlier.

In a similar way, the holding current (I_h) of the samples, which is the minimum current required to flow through the device for maintaining the ON state and which is provided by the power supply, increases with decreasing temperature, as may be observed in Fig. 4c. Higher values of the injected current are required for keeping the traps in the amorphous film filled, when the temperature decrease causes a reduction in the carrier thermal-generation rate in J_2. These results are in qualitative agreement with other published data concerning c-Si(pnpn) Shockley diodes [17].

The measured values of light triggering sensitivity at different wavelengths, for an active area of about 0.0131 cm^2, are presented in Figure 6. Figures 6a and 6b correspond to a-SiC and a-Si switches, respectively. It is obvious from all these curves that the resistivity of the c-Si(p-type) base of junction 2 (J_2) has a definite effect on the light triggering sensitivity of all samples. Reducing the resistivity of the c-Si(p-type) base results in decreased values for the light triggering sensitivity. Taking into account that the depletion region of J_2 extends mainly into the c-Si(p) region [12] (type 2 and type 4 samples), we conclude that shifting the above depletion region towards the amorphous film (type 1, type 3, and type 5 samples), by decreasing the c-Si(p) layer resistivity, results in reduced values for the light triggering sensitivity. The reason for the reduced values of light triggering sensitivity with increasing c-Si(p) base doping concentration is the decrease of the junction J_2 depletion region width, which results in the absorption of smaller amount of light within this region. Carriers generated by light can easily traverse (with no significant recombination) the J_2 depletion region if they are generated within or near the c-Si(p) depletion region (for $\lambda > 600$ nm), whereas carriers generated within the amorphous film of about 1 μm thickness (for $350 < \lambda < 600$ nm) mostly recombine before they reach the depletion region of J_2. Consequently, the maximum values of light triggering sensitivity are obtained for $\lambda = 750$ nm and $\lambda = 850$ nm for the a-SiC and a-Si switches, respectively. The maximum values of light triggering sensitivity are: $\Delta V_{BF}/\Delta P_i = 20.768$ V/mW at $\lambda = 750$ nm, and $\Delta V_{BF}/\Delta P_i = 3.4$ V/mW at $\lambda = 850$ nm, for our type 2 and type 4 samples, respectively. It should be mentioned here that the results reported in [7], for a six layer heterojunction switch using a-Si:H thin films, present only one value of light triggering sensitivity of about 5.8 V/mW at a wavelength of $\lambda = 632.8$ nm.

We observe in Figs 6a and 6b a shift of the wavelength, in which the maximum values of light triggering sensitivity are obtained, towards higher values for the a-Si switches compared with the a-SiC switches. We attribute this behavior to the higher reported values for the a-SiC energy gap ($E_{g1} = 1.36$ eV) [16], compared with the a-Si energy gap ($E_{g2} < 1$eV) [18]. The absorption coefficient (α) of a semiconductor is known [14] to be shifted at higher wavelengths as the energy gap decreases. Thus, the maximum values of light triggering sensitivity are obtained at $\lambda = 850$ nm and $\lambda = 750$ nm for the a-Si and a-SiC switches, respectively ($E_{g2} < E_{g1}$).

The higher maximum values of $\Delta V_{BF}/\Delta P_i$ also observed for the a-SiC switches compared with the a-Si switches (Figs 6a and 6b) can be attributed to the smaller

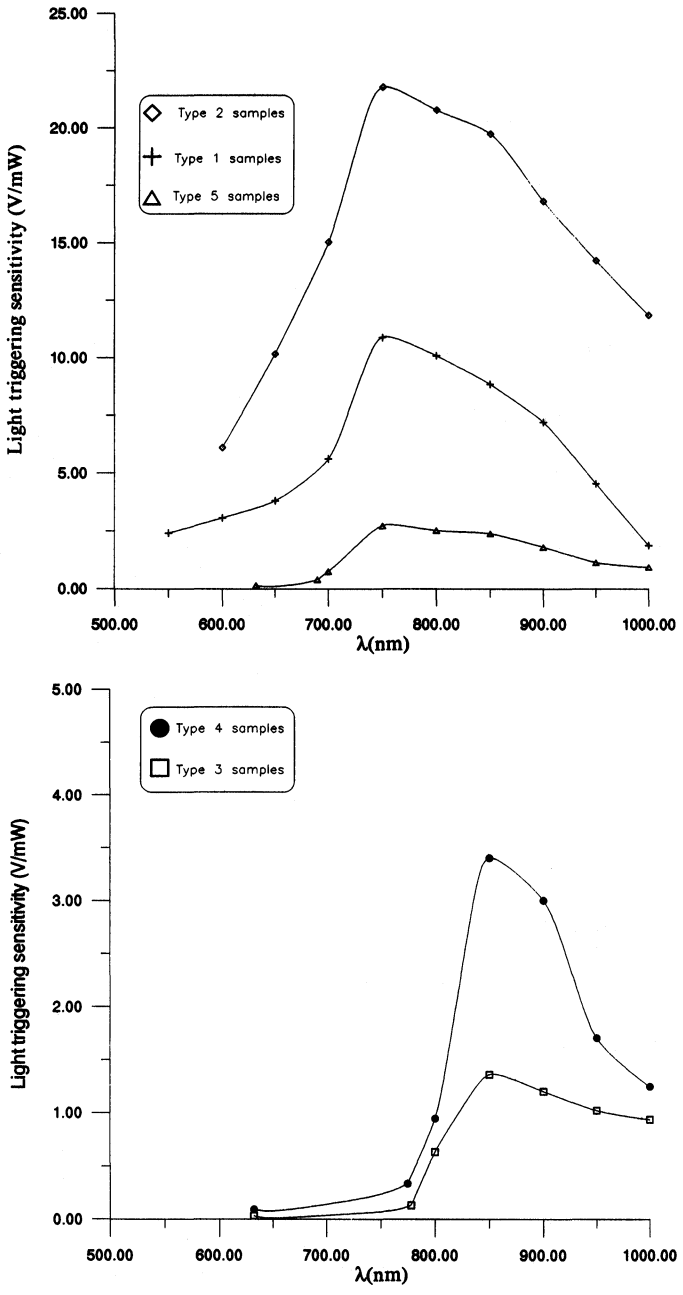

FIGURE 6 Spectral response of light triggering sensitivity of the: a) Al/a-SiC/c-Si(p)/c-Si(n^+)/Al switches, and b) Al/a-Si/c-Si(p)/c-Si(n^+)/Al switches.

reported values for the a-SiC thin films absorption coefficient (α), compared with the respective coefficient for the a-Si films [19,20]. A smaller light amount can reach junction J_2 depletion region for the a-Si switches due to the higher absorption

coefficient in the a-Si film, for generating the excess of carriers required to produce the transition to the ON state. This results in the observed smaller values of light triggering sensitivity for the a-Si switches.

The maximum values of light triggering sensitivity (Figs 6a and 6b) for type 1 and type 3 samples are significantly lower compared with the type 2 and type 4 samples, in spite of the fact that the increase in doping concentration of the c-Si(p) region is small ($\Delta N_A = N_{A(1,3)} - N_{A(2,4)} = 1.5 \times 10^{15}cm^{-3} - 6 \times 10^{14}cm^{-3} = 0.9 \times 10^{15}cm^{-3}$) compared with the respective increase for type 5 samples ($\Delta N_A' = N_{A(5)} - N_{A(1,3)} = 10^{19}cm^{-3} - 1.5 \times 10^{15}cm^{-3} = 9.998 \times 10^{18}cm^{-3}$), where $N_{A(2,4)} = 6 \times 10^{14}cm^{-3}$, $N_{A(1,3)} = 1.5 \times 10^{15}cm^{-3}$ and $N_{A(5)} = 10^{19}cm^{-3}$ correspond to the c-Si(p) base doping for type 2 and 4 samples, type 1 and 3 samples and type 5 samples, respectively. We believe that, in this case, the decrease of the c-Si(p) base width for type 1 and type 3 samples compared with that for type 2 and type 4 samples, respectively, contributes significantly to the reduced values of light triggering sensitivity, due to the smaller amount of light absorbed in the c-Si(p) base of type 1 and type 3 samples.

The switching speed of our type 1 and type 2 samples was measured and the results obtained are presented in Figure 7. Curves A and B correspond to the input square pulse and the output signal, respectively, for both types of samples. We have obtained the lowest ever reported values of rise and fall times. The rise time was about 2.7 ns and the fall time was 3 ns. Other values reported in the literature, concerning a six layer a-Si:H heterojunction [7] and a memory a-Si heterojunction bipolar switch [10], are 8 μs and 40 ns for the rise time and about submicroseconds and 200ns for the fall time, respectively.

It is known that the rise time t_r for c-Si thyristors depends [13] upon the geometric mean of the minority carrier transit times in the bases, which in our case are τ_{c1} and

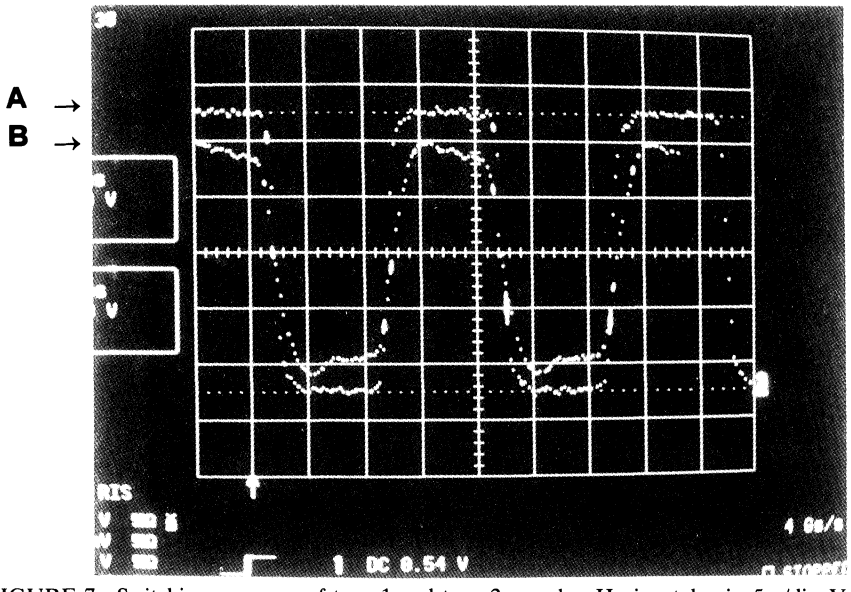

FIGURE 7 Switching response of type 1 and type 2 samples. Horizontal axis: 5ns/div. Vertical axis: 1V/div. (A → input signal, B → output signal).

τ_{c2} for the amorphous film (n-base) and c-Si(p) region (p-base), respectively, as follows:

$$t_r \propto \sqrt{\tau_{c1}\,\tau_{c2}} \tag{4}$$

and τ_{c1}, $\tau_{c2} \propto W^2$ [13], where W is the base width. Thus, the small base width of the amorphous film (1 μm) is expected to lead to low values of rise time. However, according to our model of switching transition, an excess of electrons generated within the J_2 depletion region, in avalanche breakdown conditions, causes the filling of traps in the amorphous film, and thus increases the effective carrier lifetime, especially within the J_1 depletion region. Such a trapping process is reported to occur, typically, on at most a nanosecond timescale [21], thus leading to the conclusion that such a mechanism is dominant in determining the low values of rise time measured in our samples.

The fall time t_f of the c-Si thyristors is known to be strongly affected by the minority carrier lifetime in the n-base [13], which in our case is the amorphous film. Thus, the hole lifetime in this film dominates t_f. As soon as the square pulse across the device goes from +5V to 0V, the excess of holes existing in the valence band of the amorphous film decays via recombination with trapped electrons. A hole lifetime in the order of about 10^{-8} sec, reported for a-Si:H [15], may be viewed as the upper limit for the fall time values of our non-hydrogenated a-Si and a-SiC devices.

CONCLUSIONS

The electrical and optical characteristics of high-speed amorphous switches based on a-Si/c-Si and a-SiC/c-Si heterojunctions were presented. These switches exhibit a thyristor-like behavior, and their V_{BF}, V_F, and I_h values can be reversibly controlled either by changing the light intensity falling on the samples or by affecting the sample temperature. A permanent change on V_{BF}, V_F, and I_h can also be achieved, together with a change in the high values of light triggering sensitivity, by varying the resistivity of the c-Si(p) base region. The lowest ever reported values of rise and fall times of about 3ns in these switches may prove to be of great importance in using these devices as high-speed light sensors, or high-speed optically-controlled switches.

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