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DESIGN AND ANALYTICAL STUDY OF STRAYS-INSENSITIVE SWITCHED-CAPACITOR FILTERS

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Use of analog circuit elements in active networks have become very common and the demand for their miniaturization is increasing day by day. Though several methods are available for the miniaturization of these elements through large scale integration on single chips, the performance is not very satisfactory in low-frequency applications, due to the presence of parasitic capacitance that is comparable to the capacitance of active elements. As a result, the desired response gets deviated and also noise is involved. In this paper, an attempt has been made to devise methods for the elimination or reduction of the influence of these parasitic capacitances on filter circuits.

INTRODUCTION

The use of electronic filters for selective frequency filteration has become a common application in various fields. For efficient use of these filters, it is desirable that a large number of filtering stages be fully integrated on a single IC so as to occupy as little silicon circuit area as possible.

In MOS integrated technology, it is relatively simple to achieve this objective due to the following advantages as compared to conventional techniques:

(i) high integration density.
(ii) high precision and stability.
(iii) ideal characteristics of MOSFET switches.

A more promising approach in filter design is the use of charge transfer devices (CTDs) to implement analog-sampled data transversal filters [1]. However, the performance is subjected to the following limitations: that, they are relatively inefficient in using the silicon area in implementing simple frequency response functions, the insertion losses are quite significant; and that they find it difficult to achieve the required level of noise performance with integrated MOS op-amps.

Another approach to filter design is the use of switched-capacitors (SC) circuits, which consists of op-amps and capacitors interconnected by an array of periodically operated switches. The properties offered by these circuits are low sensitivity, large dynamic range, and small physical dimensions. Furthermore, these circuits gained wide popularity due to rapid advances made in their fabrication using MOS technology. Due to these advantages, the switched-capacitor (SC) circuits are favored against the active digital and charge transfer device (CTD) filters on several occasions.

The only limitation faced by SC networks is due to the involvement of parasitic capacitances, as a result of which the actual system response deviates from the predicted one. The origin of these parasitics are mainly due to the presence of stray capacitances; finite- and frequency-dependent gain of op-amps; input voltage off sets; 'ON' resistance and junction capacitances between source, drain and substrate; effect of clock feedthrough from gate to source; and drain terminals of FETs.

The application of switched capacitors is manyfold. In many switched-capacitor realizations, a conventional analog network is taken as a basic circuit and each individual resistor is replaced by a switched-capacitor resistor. The value of resistance 'R' which is to be replaced by the switched capacitor of capacitance 'C_R' is given by

$$R = \frac{1}{f_c C_R} \tag{1}$$

where f_c = switching frequency (Fig. 1). Switched capacitors can also be used to sample a floating potential difference and provide a charge proportional to the sampled voltage. These also perform operations like additions, subtractions, and inversions and also provide delays.

A switched-capacitor network is essentially a sampled data network containing switched or unswitched capacitors and active elements such as op-amps and voltage buffers. The switching operation is carried out by the clock signal.

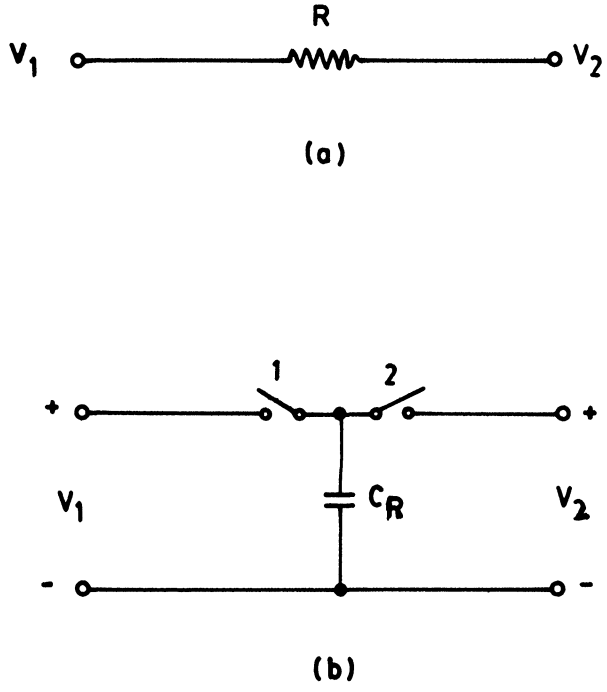


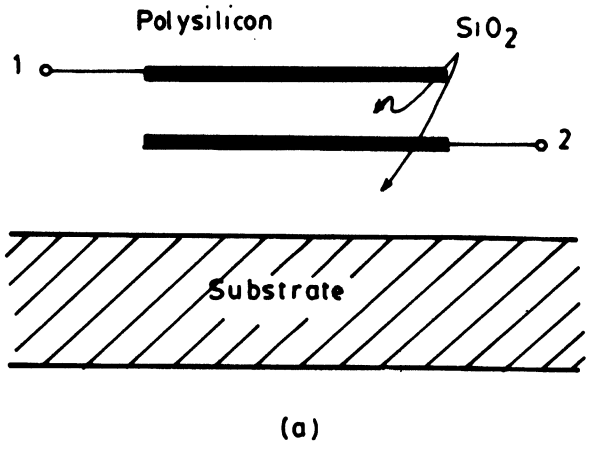
FIGURE 1 (a) The conventional analog resistor (b) Switched capacitor resistor.

In this paper the limitations of these switched-capacitor circuits are highlighted, the origin of the parasitics are carefully studied, and the effects of these parasitics on SC performance are thoroughly reviewed under some of the non-ideal candi-tions.

ORIGIN OF VARIOUS PARASITICS AND THEIR IDENTIFICATION

Parasitics resulting from the fabrication process of SWITCHED CAPACITORS:

In MOS technology, a capacitor would be fabricated as shown in Fig. 2. The nominal capacitance C_m is formed by two polysilicon layers separated by SiO_2. Owing to the technology of fabrication, there exists a parasitic capacitance C_p between the bottom plate of the capacitor C_m and the substrate as shown in the equivalent circuit of the Fig. 2.



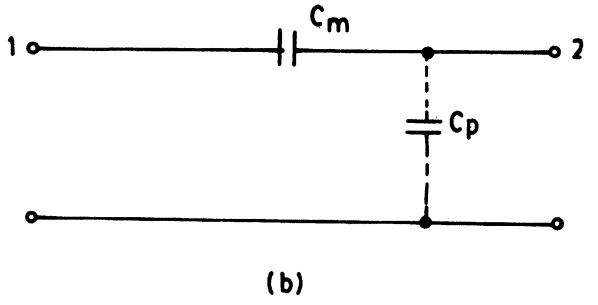


FIGURE 2 (a) A floating MOS capacitor (b) Equivalent lumped network for the MOS capacitor.

The value of C_p is usually 5% to 20% of C_m [2] and its operation may be non-linear.

Parasitics resulting from the SWITCHES

MOS switches are realized from MOS transistors. In the ON state they behave like a resistor, and like an open circuit in the OFF state. Parasitics exist between the source and drain and the substrate, which are of the order of 0.5 PF. (Fig. 3)

Parasitics due to clock feed through

Clock feedthrough is due to the capacitive coupling between gate and the channel. Due to non-linearities involved in the MOS capacitors the −ve fall time of clock feedthrough does not cancel out the +ve rise time of the clock feedthrough. Hence some parasitic capacitance is always involved in switched capacitors due to clock feedthrough.

Package parasitics

These result from lead inductances, pin capacitances, and mutual coupling between bonding leads. Therefore, the signal nodes that are electrically connected as package pins should always be either driven or at virtual ground.

EFFECTS OF VARIOUS PARASITICS ON THE FOLLOWING

Finite open loop gain of the op-amp (Fig. 4(a):

The open loop gain of the op-amp is given by $A(\delta) = \dfrac{A_o W_p}{\delta + W_p}$ (2)

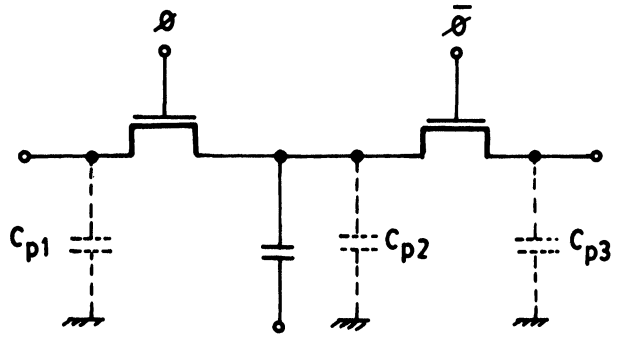


FIGURE 3 Parasitic capacitances of MOS switches.

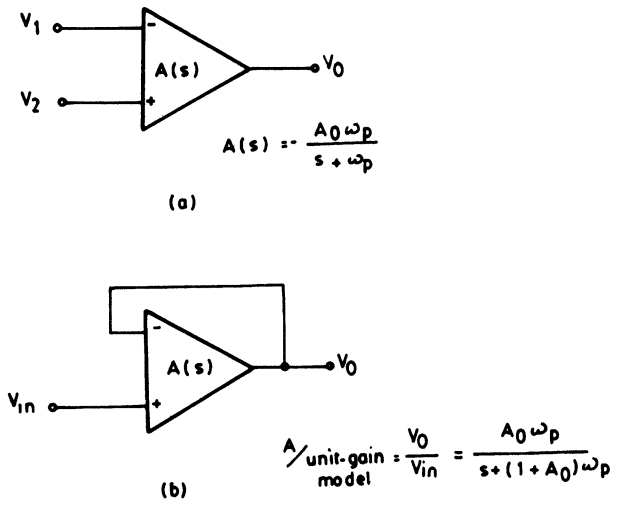


FIGURE 4 (a) An operational amplifier with finite open loop frequency dependent gain A(s) (b) Realization of unit-gain buffer by unit-gain feedback.

If the op-amp is used to realize a unity gain buffer (Fig. 4(b)) its gain will be

$$\text{A/unity gain} = V_o/V_m = A_o W_p/\delta + W_p(1 + A_o) \tag{3}$$

The characteristic equation of the above function has a pole at $p = -\omega_p(1 + A_o)$. For typical values of $f_p \cong 20$ Hz and $A_o \cong 10^5$, this pole has negligible effect on the unity gain buffer within the entire audio frequency range of operation.

Input Off set Voltage

Assuming that the input bias current of a MOS buffer is negligible, it is observed that inverting integrators are less affected by input off-set Voltage compared to non-inverting integrators.

'ON' Resistance of the Switch

At very high sampling rates, the size of the switched capacitor becomes an important consideration. The maximum permitted switching rate will be determined by the need to ensure that the capacitor charges and discharges completely during the pulse duration of the clock. This requirement sets a limit on the maximum capacitance value such that

$$\gamma_{ON} \cdot C_m \ll \frac{T}{2} \text{ is satisfied.}$$

In practice, T/2 should be about 5 times larger than $(\gamma_{on} \cdot C_m)$. Hence $C_m \leq T/10 \cdot \gamma_{on}$.

Clock feedthrough

As a result of non-linearity of the capacitors, the charges fed at the −ve and +ve transition of the clock do not cancel. This can result in a net feedthrough error voltage that has the effects similar to that of a dc offset voltage. In addition, the clock feedthrough also produces noise.

ERRORS DUE TO PARASITIC CAPACITANCE ON DIFFERENTIAL INTEGRATORS' PERFORMANCE

Switched-capacitor-based differential integrators are subjected to several important deviations from the ideal behavior (Fig. 5). For the integrating capacitor C_2, the only parasitic capacitor that affects the circuit operation is C_{p1}. The charge placed on this capacitor when input sampling switches are 'ON' is transferred on to the integrating capacitor. This results in a transfer function from input to output described by

$$V_{out} = \frac{-f_c}{JW}\left[\frac{C_1 + C_{p1}/2}{C_2} Vdm + {}^{v}_{c}m \frac{C_{p1}}{C_2}\right] \tag{4}$$

where $V_{dm} = V_1 - V_2$ and $V_{cm} = V_1 + V_2/2$

Thus, the effect of parasitic capacitance is to degrade the common mode rejection ratio (CMMR), and to change slightly the differential mode gain constant.

However, for non-inverting integration, the integrator is not affected by the parasitics. The frequency response of the switched-capacitor integrator is shown in (Fig. 6). This response deviates from the continuous one in a very different way. The inherent switching process during sampling introduces an excess phase shift at frequencies approaching the clock frequency.

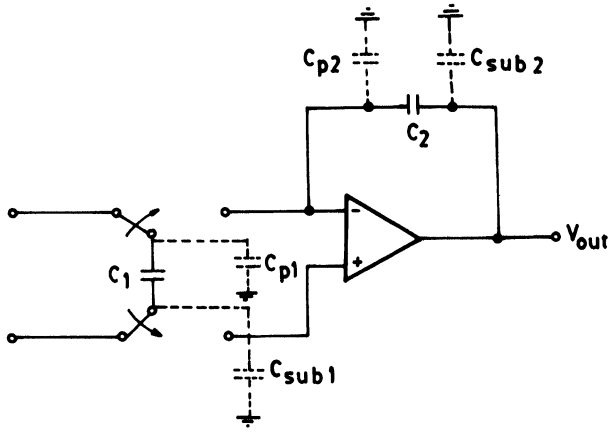


FIGURE 5 A switched capacitor differential integrator showing the parasitic capacitances associated with switches and capacitors.

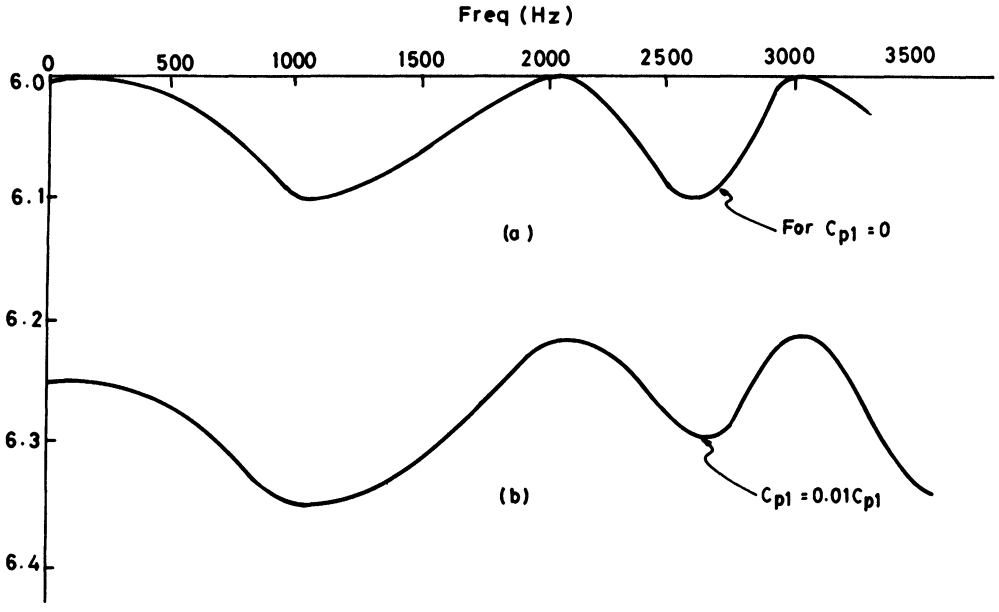


FIGURE 6 Frequency response of differntial integrator (a) Response of the circuit without parasitics (b) Response of the circuit with parasitics (c) Response of the circuit after compensation.

A straight forward analysis (over a complete clock cycle) of the switched-capacitor differential integrator gives a frequency response given by

$$H_1(W) = -\frac{C_1 f_c/C_2}{j\omega} \frac{\omega To}{2 \text{ Sin } (\omega \text{ To}/2)} \exp(-j\omega \text{ To}/2) \tag{5}$$

The first term in the brackets is the response of an ideal continuous integrator and the rest of the expression is the duration from that response caused by the sampling process. The resulting excess phase shift due to the delay term will distort the frequency response of the complete filter in a way that is similar to the effects of excess phase shift in op-amp in conventional active R-C filters. Typically, the distortion takes the form of Q—enhancement, in which the response of the filter shows some undesirable peaking.

ELIMINATION OF VARIOUS PARASITIC EFFECTS

Method—1

In this method, an attempt is made to split the parasitic capacitance into a series combination of two capacitances (Fig. 7).

One capacitance is formed between the polysilicon lower electrode and the P-well and the other between the p-well and the back gate of the substrate. Thus, the loading effect of C_{pw} on node N_2 is a minimum and C_{ws} does not affect the floating node 'N_2' at all.

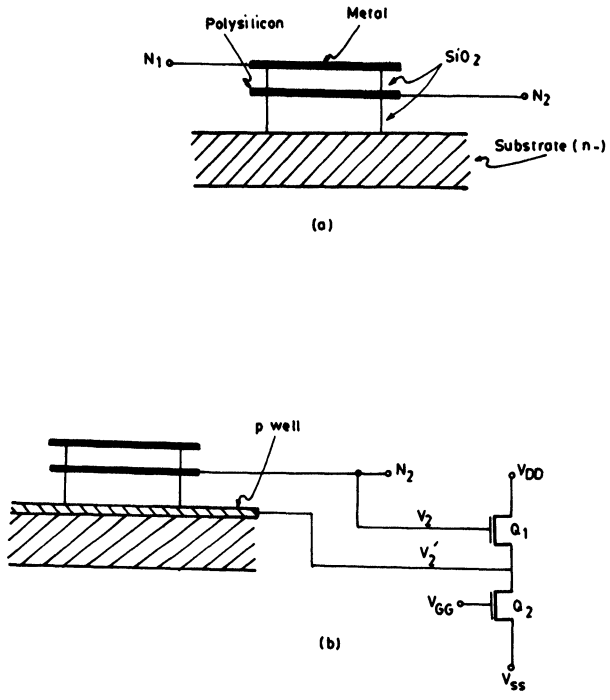


FIGURE 7 (a) Construction of a floating m.o.s. capacitor (b) Compensation scheme.

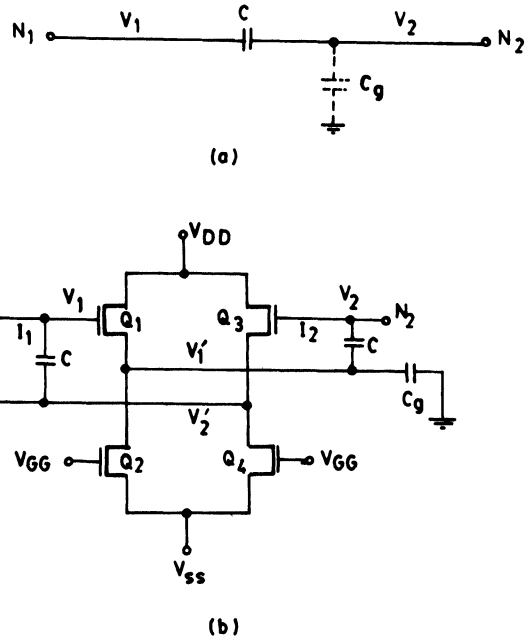


FIGURE 8 (a) Floating m.o.s. capacitor C with parasitic capacitor C_g (b) Compensating scheme.

Method—2 *(Fig. 8):*

The expression for current leaving the node N_1 is given by

$$I_1 = jwc \frac{V_1 - V_2 + V_1 (jw\, c_g + 1/R_2)/gm_1}{1 + (jw\,(C+C_g) + 1/R_2)/gm_1} \tag{6}$$

since $g^2_{m1} >> \omega^2 (C + C_g)^2 + R_2^2$

which is true for most cases. The above expression is reduced to

$$I_1 \cong j\omega c\,(V_1 - V_2) \tag{7}$$

$$I_2 \cong j\omega c\,(V_2 - V_1) \tag{8}$$

Hence the effects of 'C_g' are eliminated.

Method—3 *(Fig. 9):*

In Fig. 9, the circuit of a switched-capacitor integrator stage is illustrated. Capacitances C and C_1 together with the op-amp from the switched-capacitor frequency equivalent of an R-C active integrator. 'C_g' is the parasitic capacitance involved with 'C' and 'C_c' is the compensating capacitance.

If 'C_g' and 'C_c' are of equal value, then the net charge transferred to 'C_1' due to 'C_g' and 'C_c' becomes zero only when V_{in} is derived from a voltage source.

It is also required that 'C_c' and 'C_g' must be switched to a virtual ground in the next time interval, otherwise the compensation will not be perfect. Therefore, this scheme is somewhat restricted.

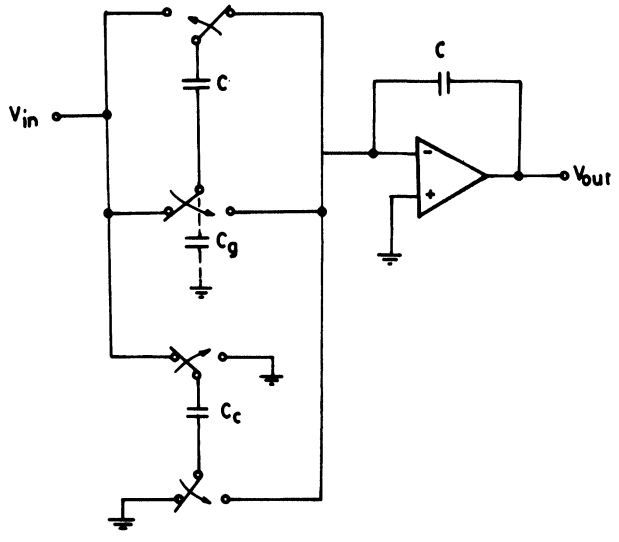


FIGURE 9 Compensated switched-capacitor or integrator.

CASE STUDY

Often in filter design, the need arises for a differential integrator that integrates the difference between the analog voltages. Here, in this case study we consider the case of an integrator (Fig. 10).

The input/output relations for the circuit are given by

$$V_{out} = -\frac{(1 + 1/R_1 C_2)}{j\omega}(V_1 - V_2) \tag{9}$$

If the same circuit is analyzed in switched-capacitor form, then the equations relating the input and output will be as per

$$V_{out} = -(f_c C_1/C_2)(V_1 - V_2) \tag{10}$$

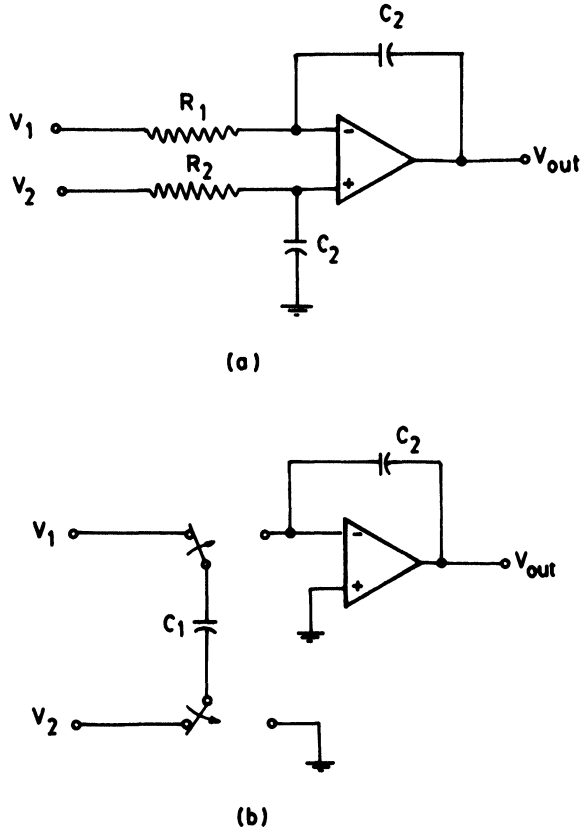


FIGURE 10 (a) A conventional differential RC integrator (b) A switched capacitor differential integrator.

The expression (10) can be modified in view of (Fig. 10) to give the form of

$$V_{out} = \frac{-f_c}{j\omega}\left[\frac{C_1}{C_2}(v_1 - v_2) + \frac{C_{p1}}{C_2}v_1\right] \tag{11}$$

and a straight forward analysis of the switched capacitor integrator gives the frequency response

$$H_1(W) = 20 \log 10\left[-\frac{1}{2j \sin(\omega T_c/2)}\frac{C_1}{C_2}\frac{C_{p1}}{C_2}\frac{V_1}{V_1 - V_2}\exp(-jwT_c/2)\right] dB \tag{12}$$

The response of this expression is plotted in Fig. 6 for different values of frequencies (200 to 4000 H_z) for two different conditions.

Condition—1

$C_{p1} = 0$, i.e., no parasitics involved.

Condition—2

$C_{p1} = 0.01\ C_1$.

The following parameters were used for the simulation of the case-study.

$T_C = 7.8125\ \mu$ sec
$T_o = 0.25\ \mu$ sec
$C_1 = 2$ pF
$C_2 = 10$ pF
$V_1 = 1050 \text{ Sin } \omega_{ct}$
$V_2 = 950 \text{ Sin } \omega_{ct}$
$\omega_c = 2\ \pi\ f_c$.

On comparison of the responses of the circuit in the presence of parasitics to that of the original circuit, we find that the gain of the integrator is distorted due to the presence of parasitics. Hence, we have to reduce the effects of parasitics for distortionless response using compensation techniques.

CONCLUSION

The origin of different type of parasitics in switched-capacitor filters and their effects on the performance of switched-capacitor filters have been discussed. Several ways of eliminating or reducing the effects of the parasitics in switched-capacitor filters are given.

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