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WIRE LAYING METHODS AS AN ALTERNATIVE TO MULTILAYER PCB'S†

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The rapid growth of integrated circuit technology, culminating in VLSI circuits, is responsible for the proliferation of new, surface mountable device packages with large numbers of input-output terminals. Conventional printed circuit or multilayer techniques have been driven to the technological edge in the effort to interconnect these new types of packages. Because the etched conductors can be replaced with fine, insulated wires, automated high density discrete wiring techniques can provide easier high density interconnections and with shorter turn-around times. Among the dozen or so presently available discrete wiring techniques, the fastest growing is Multiwire®. Multiwire is a computer based design and manufacturing system, where special machines are precisely laying down polyimide insulated wires over adhesive coated substrates having etched power and ground planes. The finished boards exhibit microstrip characteristics, providing impedance control for high speed applications. The manufacturing process and Multiwire board performance capabilities are described in this paper.

1. NEED FOR NEW INTERCONNECTION METHODS

The extremely rapid growth of integrated circuit technology is leading to an enormous increase in the number of functions implemented on a single chip. Today, we have chips containing 10,000 or even 100,000 gates and these new VLSI devices are challenging the conventional packaging and interconnection technologies which so far have been adequate for interconnection of less sophisticated MSI or LSI devices. There is a definite trend toward an increased number of I/O's, increased heat generation and faster operating speeds of these new VLSI chips. The design of adequate packages and the provision of suitable interconnections for them is becoming one of the greatest challenges for system engineers today. In addition, these new IC technologies have originated a new class of semi-custom gate array or standard logic cell IC designs permitting the user to design his unique integrated circuit within a reasonable time and at manageable cost. Frequently, these phenomena, as well as the accelerated competitive pressures drastically reduce the time to obsolescence of new products to only a few years. To remain competitive requires constant upgrading and engineering changes of existing equipment and a considerable shortening of the design cycle for new products.

The definite trend toward use of chips with an increased number of I/O's is increasing the complexity of interconnecting substrates as indicated in the table below.

This data indicates that the connective capacity of a circuit board is moving from about 30 in. of wire per square inch of substrate for a relatively simple two-sided board interconnecting DIPs, to 80 or even 200 in./in^2 for interconnecting chip carriers requiring dense multilevel conductor structures.

Board designers and manufacturers must meet these demands either by reducing the width of printed-circuit conductors and the spacing between them or by increasing the

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TABLE I
Connective capacity requirements for various packaging situations

Typical packaging situation	Approximate number of pins/in.^{2}	Amount of needed conductors (in./in.^{2})	Printed wiring levels		
			50-mil grid	24-mil grid	20-mil grid
1 16-pin dual in-line package/in.^{2}	15	34	2 (1.7)	1 (0.8)	1 (0.7)
2 16-pin DIPs/in.^{2}	30	67	3–4 (3.4)	2 (1.68)	2 (1.34)
24-pin chip-carriers on 0.5-in. center	96	216	11 (10.8)	6 (5.4)	5 (4.3)

number of conductive layers vertically. However, both choices invoke definite penalties in terms of producibility. Ensuring the integrity of hundreds of feet of 3 or 5-mil-wide conductors on the large boards or panels (up to 2 square feet) that are typically processed in the circuit-board shop – a size necessary for processing economics – is a difficult feat. Nor is the design, tooling, and manufacture of 15- or 20-layer boards a simple, high-yield process.

2. USE OF DISCRETE WIRING METHODS

Some of these circuit manufacturing pressures may be eased if the printed and etched conductors are replaced by insulated wire. The insulation in effect eliminates shorts between conductors. As a result, thin wires may be placed close to or actually in contact with each other and may cross one another without restriction on the same plane, thus considerably reducing the number of conductive planes needed for dense interconnections and greatly simplifying the design, its cost and elapsed time.

In the past decade a number of automated techniques which use insulated wire to interconnect the components have grown in popularity. There are a number of these "discrete wiring" systems available today. The most familiar is the "Wire-wrap"® system where a special tool strips insulation from the end of a wire and wraps it around a square post to form a gas tight junction. Another version is called 'quick connect'. In this technique, the wire is forced into a fork-type terminal which cuts through the insulation and provides direct contact to the wire. There is also "Unilayer", where the wire with a heat strippable insulation is point soldered to the pad or a component wire, or the "stitch-wire" system where the connection is made by first piercing the insulation by a welding tool pressure and then forming a weld between the wire and a pin or special tab on the board.

All these discrete wiring systems (and a number of additional varieties presently available) can, and are automated, but their main application remains basically for prototyping and short runs. Most of them rely on additional hardware or special areas on the board to achieve the connection of wire to components resulting in loss of surface or volumetric interconnection efficiency. Unless a "twisted pair" wiring method is used (which is difficult to automate) these discrete wiring methods cannot be successfully employed for high speed signal transmission – a growing need in todays electronics.

3. MULTIWIRE® SYSTEM

In this respect, Multiwire® boards, which also use insulated wire, are a unique system in that the wire is placed in an exact and precisely repeatable position and does not require any additional hardware to form the connection to a component, thus exhibiting the volumetric efficiency and form factors of printed wiring boards, and the electrical characteristics typical of Microstrip construction.

The Multiwire process is an automated interconnection system in which 6.3 mil, or thinner, polyimide-insulated magnet wire is laid down on an adhesive-coated substrate with etched power and ground planes. The terminations are formed by drilling through the wire and board and plating through the resultant holes. These holes are then used for component insertion and subsequent soldering operations. A cutaway view of a Multiwire board is shown in Figure 1.

If the design requires the placing of more interconnections than can be accommodated on both sides of the substrate, a layer of adhesive can be placed over the wired surface and the wiring process repeated. Thus three or even four levels of wiring patterns may be formed on a single substrate.

In the versions of Multiware boards manufactured by Fuba in Germany (as well by other licensees in Europe) surface features are incorporated by laminating a copper foil after wiring but before drilling. This allows electroplating of the through holes as well the formation of surface tabs, pads and other features in the finished product (as indicated in Figure 2). These are essential for surface mounting of VLSI packages.

The interconnecting pattern of wires is designed by the computer from the "from-to" lists supplied by the customer and this computer generated information drives the automatic wiring machine as well as a drilling machine and provides data for testing apparatus during the manufacture of the boards – a truly CAD/CAM performance. This ability to individualize the necessary logic designs through a total CAD/CAM operation permits quick introduction of engineering changes and considerably reduces, in some instances by one-half, the design cycle between completion of the logic diagram and prototype testing of the system.

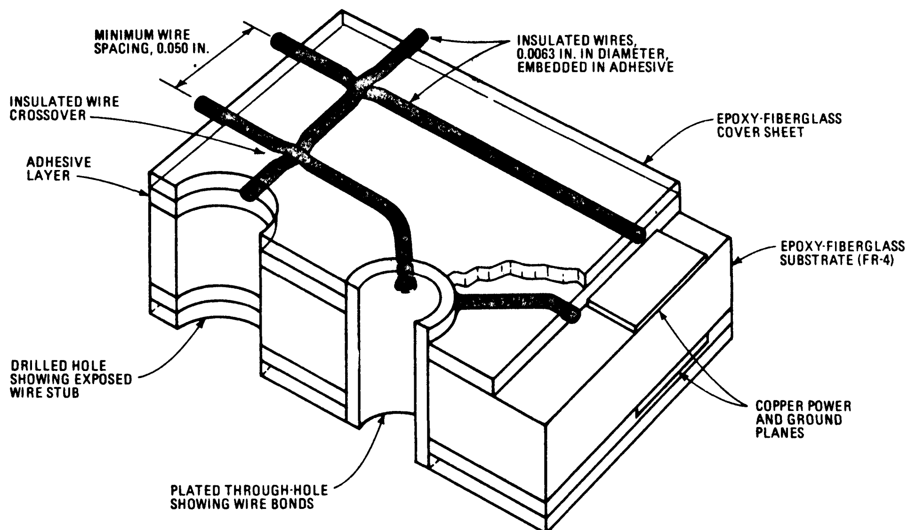

FIGURE 1 A cutaway view of multiwire board

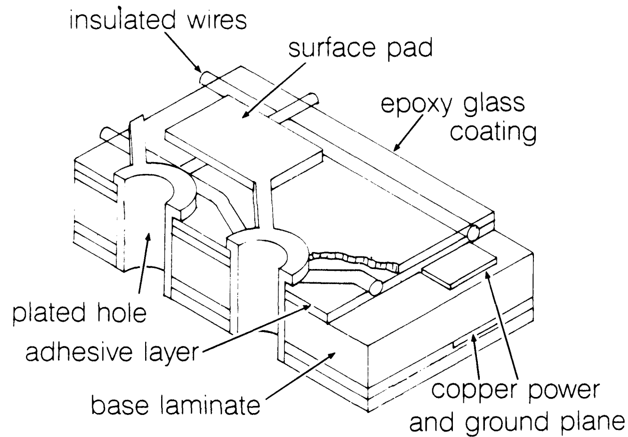

FIGURE 2 Multiwire board with surface tabs

To provide increased density of interconnections within the limited space needed to accommodate the ever increasing number of I/O's of new VLSI packages is rather a simple matter with the Multiwire System. By decreasing the grid spacing; i.e., the distance between the wireways, doubling or tripling of conductors per unit area is possible as shown in Figure 3, without greatly affecting the electrical performance, cost or delivery of the system. Further improvement could be achieved by reducing the wire diameter thus permitting even closer wire spacings without materially affecting the electrical parameters of the boards.

4. THE ELECTRICAL PERFORMANCE PARAMETERS

As the clock rates of electronic systems increase, the proper design of interconnection elements is becoming very critical in overall system performance.

The key parameters affecting the transmission properties of an interconnect are propagation velocity, characteristic impedance, and crosstalk.

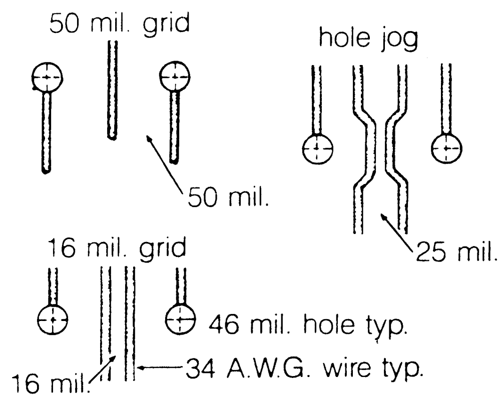

FIGURE 3 Multiwire® wiring grids

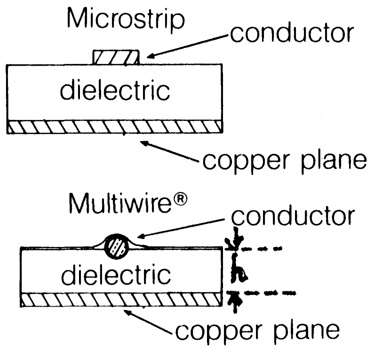

FIGURE 4 Microstrip cross sections

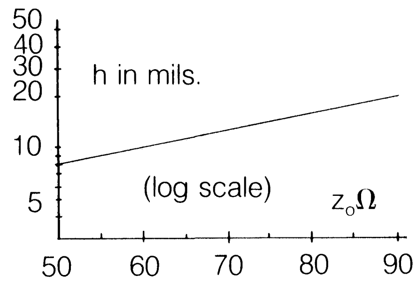

FIGURE 5 Value of Zo of Multiwire boards

a) PROPAGATION VELOCITY – Signals travelling along wires in circuit boards move about six inches (15 cm) in one nanosecond. Wave-front proportions are therefore within normal circuitboard dimensions when signal rise times are above a few nanoseconds. If conductor length can be controlled and the propagation medium held constant, then signal timing can be programmed into the interconnection design. Knowing and controlling propagation velocity is easy in planar discrete wiring.

b) IMPEDANCE CONTROL – The voltage to current relationship in a travelling wavefront is dependent on the characteristic impedance of the transmission line. The dimensions of the conductor and relative spacing of reference planes are the primary determining factors in impedance. (see Figure 4) The dielectric material is also important but to a lesser extent. In planar discrete wiring the wire itself is round and die drawn for highly accurate dimensional control. The conductor height over the reference plane can be controlled by variably spacing insulating material between the adhesive coated wiring plane and the foil underneath. (see Figure 5)

c) CROSSTALK – As the close coupling of adjacent conductors becomes the rule in high density circuit boards so the design parameters for crosstalk control should be taken into account as early as possible. Unwanted noise is generated by the electromagnetic

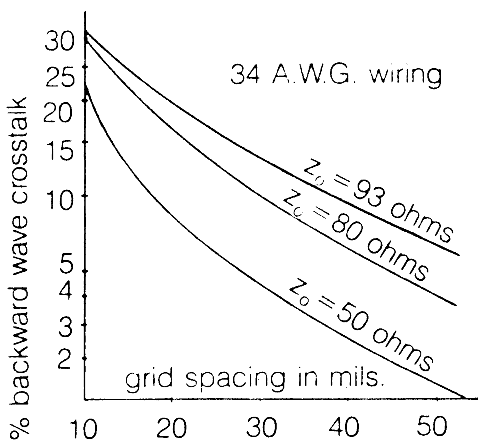

FIGURE 6 Crosstalk percentage

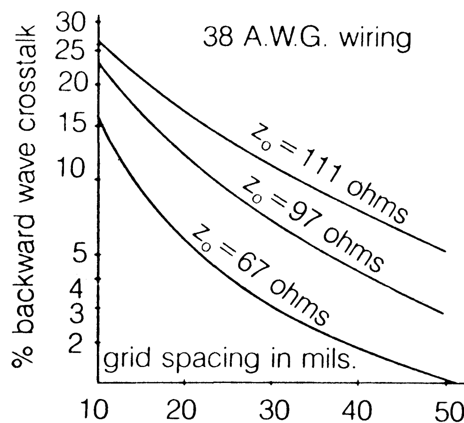

FIGURE 7 Crosstalk percentage

coupling between an active and a passive signal line. The amount of coupling is a function of the impedance between the two lines (called the mutual impedance) and the shielding provided by the proximity of a reference plane (the characteristic impedance).

There are both forward and backward waves generated in the passive line. It has been the experience of many in the design of planar discrete wiring, that if the parameters to control the backward wave are taken into account then the overall noise level will be acceptably controlled.

The following two graphs show how conductor grid spacing effects crosstalk. These graphs represent a worst case representation of the crosstalk due to the way in which the test was configured. The coupled length in all cases was well in excess of 12 inches, (30 cm) and the one nanosecond rise time pulse had enough time to complete its full voltage swing within the test region. Shorter coupled lengths would provide lower crosstalk percentages.

5. CONCLUSION

There are specific requirements in designing and prototyping high speed logic and high density VLSI packages and these are met easily by certain types of discrete wiring. Ease of change, compatability with complex electrical or mechanical design parameters that could be automated, and a manufacturing system that can be repeatable and cost effective, especially in prototype quantities, are characteristic of a discrete planar wiring system. Multiwire is such a system. The technological headroom provided by such a system will allow much further experimentation and reduced development costs.