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NEW SINGLE-CAPACITOR SIMULATIONS OF FLOATING INDUCTORS

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Out of various methods of floating inductance simulation known so far GIC-based methods of floating inductance simulation appear to be more suitable from the point of view of microelectronic application. However, a drawback of such configurations is their noncanonic nature due to the requirement of two GICs and hence two capacitors for simulating a first order impedance. This paper reports new type of FI circuits which require only one GIC and thus employ only one capacitor together with a reduced number of resistors, while retaining the merits of the usual GIC-approach.

INTRODUCTION

The importance of simulated inductors (both grounded and floating) in the context of active network synthesis is well known.[1-4] Out of various operational amplifier-RC methods of floating inductance (FI) simulation known now[5-9,11-19,24,25,27-40], those which employ two generalised-impedance-converter (GIC) type networks[5-8] have the following advantageous features from the point of view of microelectronic application:

(i) feasibility of employing low-valued capacitors compatible with microelectronic manufacturing techniques

(ii) requirement of only one component-matching condition for desired realisation and ease of adjustment for floatation by trimming a single resistance. (Note that since it is impossible to simulate a lossless FI with OA-RC networks without requiring any kind of component-matching,[20] it follows that the best configurations from this viewpoint would be those which require no more than one matching-constraint).[40]

(iii) inductance control through a single resistance and

(iv) low sensitivities to component tolerances.

The main drawback of these circuits is that two capacitors are needed to simulate a first order impedance.

Clearly, for microelectronic application[9] those FI circuits would be more suitable which, while retaining all the merits quoted above, use only a single capacitor. The purpose of this paper is to present some new FI configurations having these features.

A CIRCUIT CONFIGURATION FOR LOSSLESS FI SIMULATION

Consider the configuration of Figure 1. In analysing the circuit it is assumed that the operational amplifiers (OAs) A_2-A_4 have ideally infinite input impedance, infinite gain and zero output impedance while the DVCCS[10] A_1 has infinite input impedance and transconductance equal to G. Deleting the DVCCS A_1 and OA A_2, the rest of the circuit between terminals 1 and P can be identified as a cascade of a GIC and resistor R_4. The transmission matrix of the GIC is given by

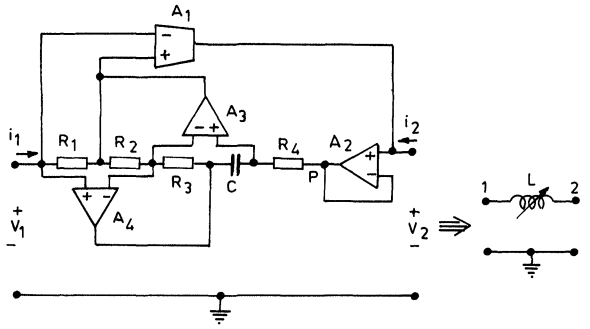

FIGURE 1 A circuit configuration for simulating a lossless floating inductance using a single GIC; $L = CR_1R_3R_4/R_2$ provided $GR_1 = 1$

$$[T] = \begin{bmatrix} 1 & 0 \\ 0 & \dfrac{R_2}{sCR_1R_3} \end{bmatrix} \tag{1}$$

Hence, the Y-matrix of the cascade of this GIC and R_4 is given by

$$[Y_1] = \frac{1}{R_4} \begin{bmatrix} \dfrac{R_2}{sCR_1R_3} & -\dfrac{R_2}{sCR_1R_3} \\ -1 & 1 \end{bmatrix} \tag{2}$$

when connecting A_2 used as a unit gain amplifier (UGA), the resulting circuit would have the Y-matrix

$$[Y_2] = \frac{R_2}{sCR_1R_3R_4} \begin{bmatrix} 1 & -1 \\ 0 & 0 \end{bmatrix} \tag{3}$$

If the DVCCS is connected as shown, it will convert the voltage across its terminals (which is equal to i_1R_1) into current Gi_1R_1 and this current will become the port-2 current i_2 of the overall 2-port network. The Y-matrix of the circuit shown in Fig. 1 is given by

$$\begin{bmatrix} i_1 \\ i_2 \end{bmatrix} = \frac{R_2}{sCR_1R_3R_4} \begin{bmatrix} 1 & -1 \\ -GR_1 & GR_1 \end{bmatrix} \begin{bmatrix} v_1 \\ v_2 \end{bmatrix} \tag{4}$$

The circuit, therefore, simulates a FI with

$$L = \frac{CR_1R_3R_4}{R_2} \tag{5}$$

provided $GR_1 = 1$ (6)

In practice, the above conditions may be achieved by adjusting the resistor R_1, such that the voltages at port 1 and 2 are indistinguishable.[11]

The following may now be noted:

(a) Like earlier GIC-based circuits,[5–8] in this case also

(i) low-valued-capacitor may be employed due to inherent capacitance-multiplication by the factor (R_4/R_2).

(ii) the circuit may be easily adjusted for floatation by trimming a single resistance R_1.

(iii) inductance value is single-resistance-tunable (with any of the resistors R_2, R_3, R_4).

(iv) all sensitivity coefficients S_i of the realised FI with respect to C_1, R_1, R_2, R_3, R_4 and G are within the range

$$0 \leqslant \| S_i \| \leqslant 1$$

(This may be verified through (4), employing the method of[11]).

(b) In contrast to earlier GIC-based circuits,[5–8] the present proposal

(i) uses only one capacitor

(ii) requires a smaller number of resistors.

COMPARISON WITH EXISTING SINGLE-CAPACITOR FI-SIMULATORS

It is useful to compare the lossless FI configuration of Fig. 1 with the single-capacitor lossless FIs employing two[19] and three[12–18] OAs.

It should be pointed out that:-

(i) whereas the circuits of[12–19] suffer from the drawback of requiring critical component-matching and consequently have pronounced sensitivity to component tolerances, the proposed circuit requires only one component-matching condition (which is adjustable through a single resistance) and has very low sensitivity.

(ii) the proposed configuration uses a smaller number of resistors (only four) than the circuits of[12–19] (which require seven to fifteen resistors).

SOME OTHER FI CIRCUITS

Many additional single-capacitance FI configurations can be derived as follows:

(i) Some interesting FI configurations, based upon nonideal GICs derived from the circuits of,[21–23] are shown in Fig. 2. Note that these circuits have the novel feature of employing a minimum possible number of passive components (i.e. one capacitor and two resistors) although they simulate lossy FIs with floating immittances given by $Z(s) = R_s + sL$ or $Y(s) = 1/R_p + 1/sL$.

(ii) Entirely OA-based versions of the circuits of Fig. 1 and 2 may be obtained by replacing the DVCCS with one OA and five resistors, but these would use more numbers of resistors and would require additional realisation constraints to be fulfilled.

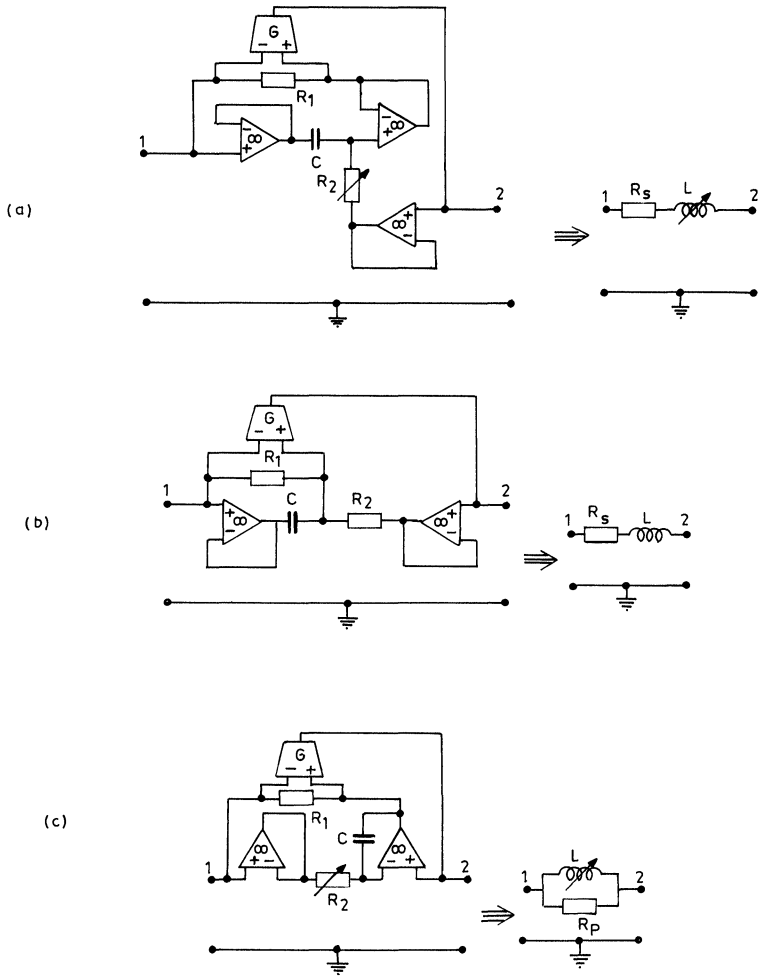

FIGURE 2 Some configurations for simulating lossy floating inductors (a) $R_s = R_1$, $L = CR_1R_2$ (b) $R_s = R_1 + R_2$, $L = CR_1R_2$ (c) $R_p = R_1$, $L = CR_1R_2$. In all cases the condition of simulation is $GR_1 = 1$.

(iii) Many other variants of the proposed circuits and those outlined in (ii) may be obtained by replacing the OAs by nullator-norator pairs and then recomponsing the circuits by alternative grouping of nullators and nurators to form ideal OAs.

REALISATION OF FLOATING FDNR AND FDNC ELEMENTS

A variety of floating FDNR and FDNC type immitances[26] may be realised by alternative choice (resistive/capacitive) of passive components in the circuits of Fig. 1 and 2 (and those outlined above). However, a particularly promising configuration for this purpose is that of Fig. 1. The circuit would simulate a floating FDNR $Z(s) = 1/Ds^2$ if resistors R_3 and R_4 are replaced by capacitors C_3 and C_4 and the capacitor is replaced by a resistor R; $Z(s) = R_1/s^2C_3C_4R_2R$. Similarly, a floating FDNC $Z(s) = Ms^2$ would be realisable by

replacing R_2 by a capacitor C_2 while keeping all other components as they are; thus giving $Z(s) = s^2CC_2R_1R_3R_4$.

Note that in contrast to previously known GIC-based floating FDNR/FDNC realizations[8] which would employ four OAs five resistors and four capacitors, the suggested circuits (a) employ only two capacitors and hence are canonic (b) use only three resistors. In both cases, simulated elements are single-resistance-tunable.

CONCLUSIONS

A circuit configuration is presented for lossless FI simulation and it retains the characteristic features of the earlier two-GIC-based approaches to FI simulation but by contrast, requires a single GIC and hence (i) employs only a single capacitor, thus, requiring 50% less total-capacitance compared to earlier circuits[5–8] for the same value of inductance (ii) requires a smaller number of resistors. Also, a few circuits employing non-ideal GICs are presented which simulate lossy FIs and have the novel feature of requiring a minimum possible number of passive elements. The characteristic advantages of the proposed circuits are retained when they are used to realise FDNR or FDNC type floating immittances through alternative choice of circuit impedances.

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