Electrocomponent Science and Technology, 1982, Vol. 10, pp. 1-6
0305-3091/82/1001-0001 $6.50/0

DIRECT CHIP MOUNTING — A CHALLENGE TO THE DESIGN ENGINEER†

J. LORMAN and J. PROCHASKA
RSISFE, Prague, Czechoslovakia

(Received November 11, 1981; in final form April 3, 1982)

The extrapolation of development trends in the area of technologically complicated electronic equipment shows an ever increasing complexity in semiconductor technology. This development has so concerned the constructors of electronic equipment that progress in the technology of mounting and interconnection has taken a secondary place.

This growing divergence between a fast developing microelectronic industry, and a conservative state of the macroelectronics industry, is a driving force with regard to the progress to effective connection technologies at every level of mounting. The technological solution to all systems will then become more coordinated.

The mounting of components to printed circuit boards is traditionally a soldering operation. This principle lead to the development of full automation, and is a standard mounting technology. The growth of integration at the chip level has however brought new requirements that are only satisfied with difficulty.

Newly developed requirements show that the use of dual-in-line packages will be unsatisfactory. New methods must be designed to connect the chips directly to the printed circuit board, going from the chip as the smallest mounted unit.

Requirements for very complex electronic equipment with a high degree of integration (LSI or VLSI) are not satisfied using traditional mounting systems. These require a totally new mounting concept, from the chips to the printed circuit board.

In this paper alternatives to printed circuit board technology with insulated wiring (multilayers), and the mounting of chips from film carriers, are evaluated. These principles have a good possibility of further improvement as progress in mounting technology continues.

Price reductions cause an extension of application possibilities and an extension of electronic designs. It is harder to make choices for new designs when there are more degrees of freedom. However the function of chips as the basic element is unchangeable and optimum designs need to be based on this concept.

INTRODUCTION

An extrapolation of development trends in the field of computing technology shows the semiconductor level continuing to grow in importance. There seems no reason to doubt that this trend, which has been apparent for about the last fifteen years, will be maintained for at least the next ten years. Convincing support for this view is provided by the graph showing the shrinking size of minimum features on the chips as a function of time (Figure 1).[1]

So pleased were the designers of electronic systems with this development that progress in the mounting and wiring of these components came to be regarded as of secondary importance. The resultant disparity between, on the one hand, the rapid development on the microelectronic level and, on the other hand, the conservative state of wiring technology, became a motive force of research and development aimed at providing more effective wiring techniques at all levels of assembly. In other words, endeavours are orientated towards finding a harmonised technological solution for the entire functional system.

†Paper first given at Electronica, Munich, 1980. First received in English form 10.11.80 and in final form. 3.4.82.

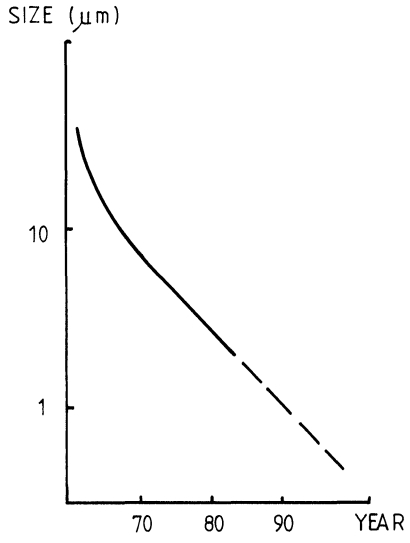

FIGURE 1 Size of minimum feature on chips as a function of time.

In what area, then, do we find these endeavours being concentrated? If we concede the dominance of the microelectronic level, then the answer is: in the area of the IC package and its mounting. A growing number of logical elements on the chip demand corresponding interconnections, both internal (increased relationship of interconnection area to logic contained on the chip), and external (increased number of leads). Study[1] makes the following predictions for the year 1990: a relationship of wiring area to logic contained on chip of at least 2 : 1, and up to 200 terminals (Figures 2 and 3). Under such circumstances the external wiring of the chips (i.e. design of packages and pc boards) requires a thoroughgoing innovation. Among the points contained in studies 3 and 4 is the fact that an increase in the number of terminal pins per unit area of pc board must lead to a major rise in the number of signal layers.

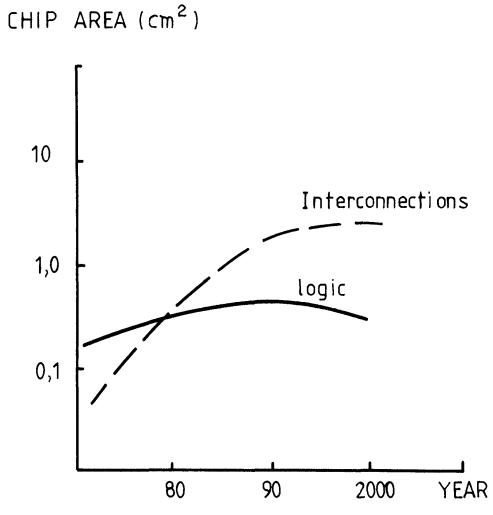

FIGURE 2 Chip area as a function of time.

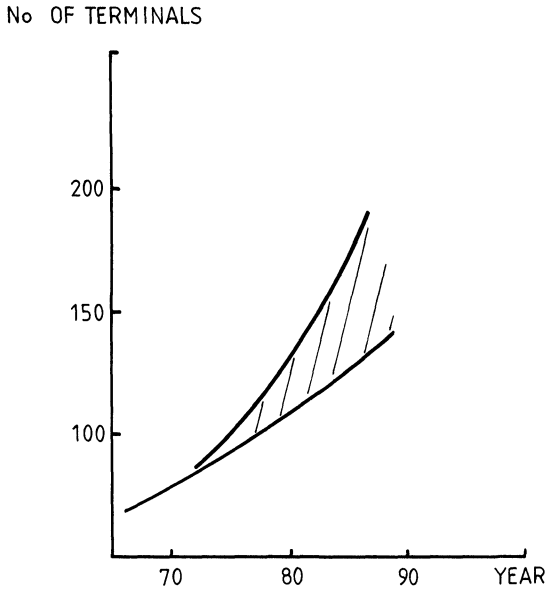

FIGURE 3 Number of terminals as a function of time.

Pins spaced at intervals of 2.54 mm entail 4 signal layers, while, with a wiring grid on the pc board of 1.27 mm, a pin spacing of 1.27 mm raises the requirements to 11 layers (Figure 4). If the pins are distributed across the entire underside of the package at intervals of 1.27 mm it proves necessary (assuming a similar grid on the pc board) to have 20 conductive layers. However, such solutions are economically quite unacceptable, since it

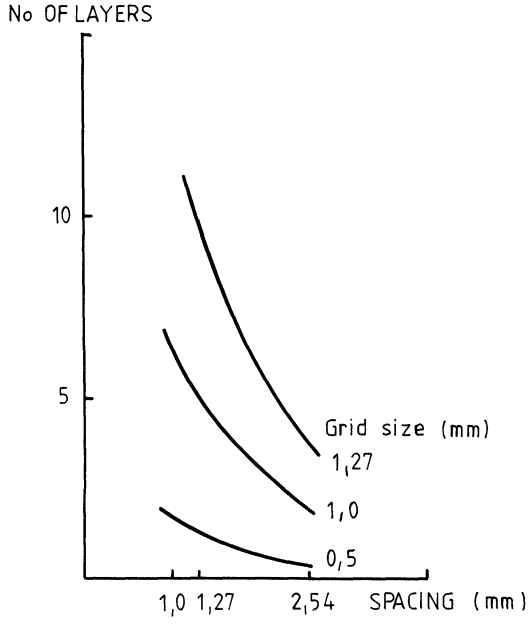

FIGURE 4 Number of layers as a function of spacing for various grids.

is necessary that the increasing packing costs density, or falling costs per bit, be accompanied by a reduction in costs for the external wiring (i.e. for the mounting). The mounting and wiring techniques so far employed cannot possibly meet this requirement.

PRINTED CIRCUITS AND THEIR POSSIBILITIES

While not rejecting multilayer pc boards, we are very conscious of the high expenditure involved, which rises progressively with increasing density. We consider it possible that the exploitation of this technique must be left to the sphere of fully automated large-scale production.

One notable advance is Multiwire technology. Since this technology permits the crossing of insulated wires in one plane, a roughly fivefold increase in interconnection density becomes realisable.[4] The cost involved are equivalent to those for a 4-plane pc board with a wiring grid of 1.27 mm. Raising interconnection density per unit area by the use of further layers or by concentrating the wiring grid (down to 0.45 mm) is also possible in combination with Multiwire technology, although this entails an increase in the cost of producing each pc board. Even so, the technology of pc boards using insulated wires as conductive paths appears to us to represent a striking qualitative change, particularly as regards its versatility.

MULTICHIP MODULES

A further area of development in which improved cost-effectiveness can probably be expected is at the level of the IC package. We would like to deal with this aspect by quoting a few of the points raised by study:[3] A 90% conversion of circuits with DIP's into LSI chips in chip-carrier packages (this represents the optimal way of constructing a processor in a medium-sized computer) results in a 50% reduction in system costs. A complete conversion of circuits with DIP's into SSI and LSI chips, using a hybrid wiring pattern in the package, lowers system costs by as much as 70%. Thus, one way of dealing with increased density is with multichips – a second qualitative change.

MOUNTING: A NEW GENERATION

The direction of development at the level of pc board and package is prescribed, first and foremost, by the demands of design and technology, as well as by the economic considerations resulting from these demands. Even though this trend represents a qualitative advance, it does not imply a compulsion to respect the development of the system's functional parameters with regard to a large reserve. A more advanced conception of this reserve approaches the point at which one may begin to speak of the advent of a new generation. The most pressing problems are likely to be those of heat removal. If, with growing integration density of special logic on the chip, the number of pins is to be kept at a reasonable level (this condition being imposed on us by the expected external interconnection problems), then we come up against an obstacle: how is heat to be conducted away from the chip? The increasing interconnection density on the chip, accompanied by a reduction of the diameter of the wiring paths, leads to increased radiation of heat. The limit for an air-cooled package is 1 W/cm^2.

We consider the following two principles as points of departure for a solution to this problem:

– shortening the interconnections between logical elements (concentration of volume),

– cooling by means of liquids or liquefied gases (cryogenic principles).

These two principles are essentially interconnected. Obviously, the solution which prevails in this area will be one representing a design form which respects the chip as an elementary building block. In this connection, the concept "direct mounting of chips" arises as an operational description of a new generation in mounting technology.

DIRECT MOUNTING OF CHIPS

The most widespread form of direct mounting is the integrated hybrid circuit, particularly in its multichip version.[6] In this case, the main advantage is a great flexibility in design. On the other hand, the actual chip connection by means of flying leads must be considered a drawback. The most important technico-economic problem is the fact that a growing number of chips on the substrate is accompanied by a progressively falling yield.

In this respect, the technology of spider-bonding represents an advance. Here, the network with the chip in itself constitutes a package;[8] also, a complete input test can be carried out. The robust construction of the leads also permits direct mounting onto the pc board.

Another approach to the problem of concentrating the mounting is ST* technology,[7] in which the chips are wired onto the substrate by means of layers applied by the additive process. The resulting assembly is relatively robust, but cannot be repaired, and has the disadvantage of a low yield.

So the attempts to mount the chips directly are by no means new. Surmounting the obstacle presented by the modular function of the chip-pc board interface (chip-package-pc board) becomes the criterion of success. A reserve – in a vertical direction – for the purposes of diagnostic inputs and repair seems to be indispensible. The abandonment of this reserve could only be considered if there were a high yield or low costs for the resulting assembly complex. By providing the technological solution, we should be helping to see that at least one of these preconditions is fulfilled.

The simplest answer seems to be a dividing-up of the system into section – modules. The external connection of the module retains the mounting, including the existing power supply and cooling.

Considering the number of terminals required (about 100), a matrix configuration of the axial pins seems realistic. The internal structure of the module should enable the chips to be built up vertically on top of each other. At the same time there is the possibility of combining the semiconductor chips and the connecting chips. Figure 5 offers

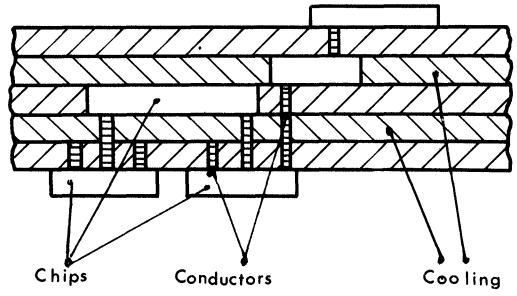

FIGURE 5 Structure of module.

*Semiconductor – Thermoplastic – Dielectric.

a view of such a construction. The modular space between the chips is filled with a coolant. Obviously, such a concept of "multilayer" modules requires the configuration of the contact surfaces and the typology of the interconnection patterns to be highly unified. An additional precondition is the complete automation of the production process, from design to testing, including in-circuit testing.

EVALUATION

If we accept the chip and pc board as two basic constructional levels – and this standpoint is justified both with regard to the specific technological frames of reference of both levels, and from the system construction aspect – then we still find, existing side by side, a whole range of variants and intermediate stages. Once the choice has been made from among these variants, a way can be found to optimally meet the demands imposed on the designed system.

The applications, and thus the conditions and aims governing the design of electronic installations, become broader. At same time there is a steady fall in the price of the basic components. The scope for the design – at higher levels – is extended. The design engineer is given a greater degree of freedom, but also constantly changing criteria as regards costs.

However, the function of the chip as a basic component does not change. The optimal design should always have this component as its point of departure.

REFERENCES

1. Electronics **53** pp 531-563 1980.
2. J. Lyman, Electronics **51** pp 117-125 1978.
3. D. Amey, Electronics **53** pp 113-117 1980.
4. R. Burr, Electronics **52** pp 117-121 1980.
5. R. Hornlein, Fachsitungsprogramm *Productronica* 1979.
6. J. Lyman, Electronics **49** pp 92-104 1976.
7. R. Clark, *Proce. ISHM Symp.* pp 131-144 1974.
8. J. Smith, *IEEE Trans. on PHP* – **10** pp 257-268 1977.
9. A. Durniak, Electronics **52** pp 111-133 1979.