

Research Article

High-Input Impedance Voltage-Mode Multifunction Filter with Four Grounded Components and Only Two Plus-Type DDCCs

Hua-Pin Chen

Department of Electronic Engineering, Ming Chi University of Technology, Taishan 243, Taiwan

Correspondence should be addressed to Hua-Pin Chen, hpchen8888@xuite.net

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This paper introduces a novel voltage-mode multifunction biquadratic filter with single input and four outputs using two plus-type differential difference current conveyors (DDCCs) and four grounded passive components. The filter can realize inverting highpass, inverting bandpass, noninverting lowpass, and noninverting bandpass filter responses, simultaneously. It still maintains the following advantages: (i) using grounded capacitors attractive for integration and absorbing shunt parasitic capacitance, (ii) using grounded resistors at all X terminals of DDCCs suitable for the variations of filter parameters and absorbing series parasitic resistances at all X terminals of DDCCs, (iii) high-input impedance good for cascadability, (iv) no need to change the filter topology, (v) no need to component-matching conditions, (vi) low active and passive sensitivity performances, and (vii) simpler configuration due to the use of plus-type DDCCs only. HSPICE and MATLAB simulations results are provided to demonstrate the theoretical analysis.

1. Introduction

As a current-mode active device, the differential difference current conveyor (DDCC) has the advantages of both the second-generation current conveyor (CCII) (such as large signal bandwidth, great linearity, wide dynamic range) and the differential difference amplifier (DDA) (such as high-input impedance and arithmetic operation capability) [1]. This element is a versatile building block whose applications exist in the literature [1–7]. Voltage-mode active filters with high-input impedance are of great interest because several cells of this kind can be directly connected for implementing higher-order filters [3–11]. In 2003, Chang and Chen proposed a universal voltage-mode filter with three inputs and a single output [2]. The circuit can realize all five different generic filtering responses but only highpass and bandpass responses have the advantage of high-input impedance. In 2004, Horng et al. proposed a multifunction filter with a single input and three outputs [3]. The circuit can realize highpass, bandpass, and lowpass responses, simultaneously. However, it is based on two minus-type DDCCs. In 2005, Ibrahim et al. proposed two single DDCC

biquads with high-input impedance and minimum number of passive elements [4]. The highpass, bandpass, or lowpass filter responses cannot be realized in the same configuration. In 2007, Chiu and Horng proposed a universal voltage-mode filter with three inputs and a single output [5]. The circuit has high-input and low-output impedance advantages but it uses three plus-type DDCCs. In the same year, Chen proposed a universal voltage-mode filter based on two plus-type DDCCs [6]. The proposed configuration suffers from high-input impedance. Recently, Horng proposed another universal voltage-mode filter with three inputs and five outputs [7]. However, it still uses three plus-type DDCCs. In this paper, a new voltage-mode multifunction biquadratic circuit with single input and four outputs is presented. The proposed circuit employs only two plus-type DDCCs, two grounded capacitors, and two grounded resistors. It has the same advantages reported by Horng et al. [3], such as realization of highpass (HP), bandpass (BP), and lowpass (LP) filter responses from the same configuration, no requirements for component-matching conditions, the use of only grounded capacitors and resistors, high-input impedance, and low active and passive sensitivity

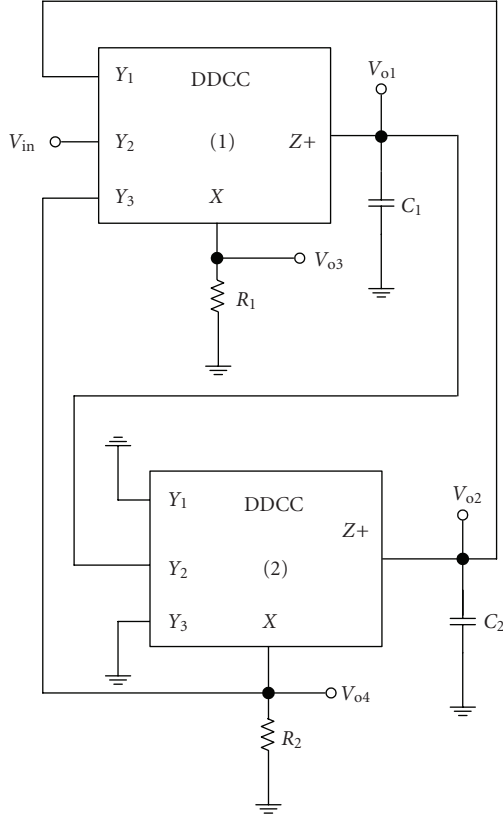


FIGURE 1: The proposed high-input impedance voltage-mode multifunction biquad based on plus-type DDCCs.

performances. Moreover, the proposed circuit is simpler in configuration than the old circuit, since the use of only plus-type of DDCC is simpler than minus-type one like a CCII [11].

2. Circuit Description

The DDCC is a five-terminal analog building block and its terminal relations are given by $I_{Y1} = I_{Y2} = I_{Y3} = 0$, $V_X = V_{Y1} - V_{Y2} + V_{Y3}$, and $I_Z = I_X$ [1]. The proposed multifunction biquadratic circuit comprises two plus-type DDCCs, two grounded capacitors, and two grounded resistors, as shown in Figure 1. The use of grounded capacitors makes the circuit suitable for integration because grounded capacitor circuit can compensate for the stray capacitances at their nodes [12, 13]. Derived by each nodal equation of the proposed, the input-output relationship matrix form of Figure 1 can be expressed as

$$\begin{bmatrix} sC_1 & 0 & -G_1 & 0 \\ G_2 & sC_2 & 0 & 0 \\ 1 & -1 & 1 & 0 \\ 1 & 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_{o1} \\ V_{o2} \\ V_{o3} \\ V_{o4} \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ -V_{in} \\ 0 \end{bmatrix}, \quad (1)$$

where $G_1 = 1/R_1$ and $G_2 = 1/R_2$.

To derive (1), all the Y_1 , Y_2 , and Y_3 terminals of DDCC are high-impedance terminals, since they are connected to

gates of MOS devices in actual implementation, whereas the port X is low-impedance terminal [1]. Similarly the port $Z+$ also exhibits high impedance since it is connected to the output stage of current mirror. From (1), the following four output voltages can be derived as

$$\begin{aligned} \frac{V_{o1}}{V_{in}} &= \frac{-sC_2G_1}{s^2C_1C_2 + sC_2G_1 + G_1G_2}, \\ \frac{V_{o2}}{V_{in}} &= \frac{G_1G_2}{s^2C_1C_2 + sC_2G_1 + G_1G_2}, \\ \frac{V_{o3}}{V_{in}} &= \frac{-s^2C_1C_2}{s^2C_1C_2 + sC_2G_1 + G_1G_2}, \\ \frac{V_{o4}}{V_{in}} &= \frac{sC_2G_1}{s^2C_1C_2 + sC_2G_1 + G_1G_2}. \end{aligned} \quad (2)$$

Thus, we can obtain an inverting BP, a non-inverting LP, an inverting HP, and a non-inverting BP filter response at the output voltages; V_{o1} , V_{o2} , V_{o3} , and V_{o4} , respectively. In order to realize allpass and bandstop filter functions, the unity gain voltage difference amplifier is needed. Due to the fact that input voltage signal is connected directly to the Y_2 port of the DDCC(1) and input current to the Y_2 port is zero, the circuit has the feature of high-input impedance. The employs of only plus-type DDCCs simplify the circuit configuration.

The resonance angular frequency ω_o , quality factor Q , and bandwidth BW are given by

$$\omega_o = \frac{1}{\sqrt{R_1R_2C_1C_2}}, \quad Q = \sqrt{\frac{R_1C_1}{R_2C_2}}, \quad BW = \frac{\omega_o}{Q} = \frac{1}{R_1C_1}. \quad (3)$$

Equation (3), the parameters ω_o , and BW can be orthogonally adjusted by resistor R_1 while the orthogonal tuning ω_o and Q can be achieved by simultaneous adjustment of R_1 and R_2 such that $R_1 = R_2$. It must be noted that the use of grounded resistors in the proposed circuit will benefit by an easier electronic tunability. Thus, for the case of $R_1 = R_2$ can be solved by using two MOSFETs to replace R_1 and R_2 with its gate connected by the same voltage control [14, 15]. Several realizations of tunable grounded resistors exist in the literature [16, 17].

3. Effect of Nonidealities

Take into account the nonidealities of a DDCC, namely, $V_X = R_X I_X + \beta V_{Y1} - \gamma V_{Y2} + \eta V_{Y3}$ and $I_Z = \alpha I_X$, where R_X , α , β , η , and γ are the intrinsic resistance at the X terminal, the parasitic current gain at the X terminal to the Z terminal, the parasitic voltage gain at the Y_1 terminal to the X terminal, the parasitic voltage gain at the Y_2 terminal to the X terminal, and the parasitic voltage gain at the Y_3 terminal to the X terminal, respectively. These parasitic components limit the

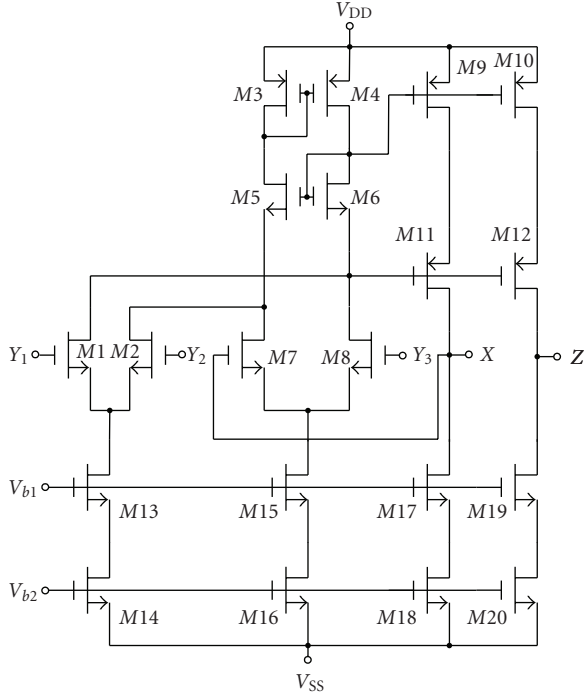


FIGURE 2: CMOS implementation of the plus-type DDCC.

high-frequency operation of the circuit and can be modeled with the following first-order functions [18]:

$$\begin{aligned}\alpha &= \frac{\alpha_o}{1 + \tau_\alpha s}, \\ \beta &= \frac{\beta_o}{1 + \tau_\beta s}, \\ \gamma &= \frac{\gamma_o}{1 + \tau_\gamma s}, \\ \eta &= \frac{\eta_o}{1 + \tau_\eta s}.\end{aligned}\quad (4)$$

In (4), the pole frequencies $\omega_\alpha = 1/\tau_\alpha$, $\omega_\beta = 1/\tau_\beta$, $\omega_\gamma = 1/\tau_\gamma$, and $\omega_\eta = 1/\tau_\eta$ depend on the technological parameters and ideally approach infinity. The operation frequency of the presented filter can be defined as $f \ll \min\{\omega_\alpha, \omega_\beta, \omega_\gamma, \omega_\eta\}$. In addition, the dc gain α_o , β_o , γ_o , and η_o are ideally equal to unity and can be expressed as $\alpha_o = 1 - \varepsilon_\alpha$, $\beta_o = 1 - \varepsilon_\beta$, $\gamma_o = 1 - \varepsilon_\gamma$, and $\eta_o = 1 - \varepsilon_\eta$, where ε_β , ε_γ , and ε_η are the voltage tracking errors, and ε_α is the current tracking error in addition to $|\varepsilon_\beta| \ll 1$, $|\varepsilon_\gamma| \ll 1$, $|\varepsilon_\eta| \ll 1$, and $|\varepsilon_\alpha| \ll 1$. Taking into account the nonidealities, the denominator of the transfer functions of Figure 1 becomes

$$D(s) = s^2 C_1 C_2 + \alpha_{o1} \eta_{o1} \gamma_{o2} s C_2 G'_1 + \alpha_{o1} \alpha_{o2} \beta_{o1} \gamma_{o2} G'_1 G'_2. \quad (5)$$

The nonideal resonance angular frequency ω_o and quality factor Q are obtained by

$$\omega_o = \sqrt{\frac{\alpha_{o1} \alpha_{o2} \beta_{o1} \gamma_{o2} G'_1 G'_2}{C_1 C_2}}, \quad Q = \frac{1}{\eta_{o1}} \sqrt{\frac{\alpha_{o2} \beta_{o1} C_1 G'_2}{\alpha_{o1} \gamma_{o2} C_2 G'_1}}. \quad (6)$$

A sensitivity study forms an important index of the performance of any active network. The formal definition of sensitivity is $S_x^F = (x/F)(\partial F/\partial x)$, where F represents one of ω_o , Q and x represents any of the elements ($G'_1 - G'_2$, $C_1 - C_2$) or the active parameters (α_i , β_i , γ_i , η_i). Based on the sensitivity expression, the active and passive sensitivities of the proposed circuit shown in Figure 1 are given as

$$\begin{aligned}S_{\alpha_{o1}, \alpha_{o2}, \beta_{o1}, \gamma_{o2}}^{\omega_o} &= S_{G'_1, G'_2}^{\omega_o} = -S_{C_1, C_2}^{\omega_o} = \frac{1}{2}, \\ S_{\alpha_{o2}, \beta_{o1}}^Q &= S_{C_1, G'_2}^Q = -S_{\alpha_{o1}, \gamma_{o2}}^Q = -S_{C_2, G'_1}^Q = \frac{1}{2}, \\ S_{\eta_{o1}}^Q &= -1.\end{aligned}\quad (7)$$

Hence, the filter parameter sensitivities are low and not larger than unity in absolute value.

4. Simulation Results

The device model parameters used for the HSPICE simulations are TSMC 0.35 μm CMOS 2P4M process and MATLAB for the theoretical part to compare the results. The CMOS implementation of the differential difference voltage current conveyor is shown in Figure 2 [4]. The NMOS and PMOS transistor aspect ratios are given by $W/L = 2.5 \mu\text{m}/0.5 \mu\text{m}$ and $W/L = 10 \mu\text{m}/0.5 \mu\text{m}$, respectively. The supply voltages are $V_{DD} = -V_{SS} = 1.65 \text{ V}$, and the biasing voltages of V_{b1} and V_{b2} are -0.1 V and -0.8 V , respectively. The proposed circuit was designed for $f_o = 1 \text{ MHz}$ and $Q = 1$ by choosing $R_1 = R_2 = 50 \text{ k}\Omega$ and $C_1 = C_2 = 3.18 \text{ pF}$. Figure 3 shows the simulated results amplitudes for HP, LP, and two BP filter responses of Figure 1. The total power dissipation is found to be 0.52 mW . As can be seen, there is a close agreement between theory and simulation.

The noise behavior of the filter was simulated using the INOISE and ONOISE statements of frequency responses of the BP response at V_{o4} output terminal. Figure 4 shows the simulated amplitude-frequency responses for the BP filter with INOISE- and ONOISE-designed $R_1 = R_2 = 31.8 \text{ k}\Omega$ and $C_1 = C_2 = 5 \text{ pF}$. The total equivalent input and output noise voltages are 13.8 mV and 0.48 mV , respectively.

To test the input dynamic range of the filter, the simulation has been repeated for a sinusoidal input signal at $f_o = 1 \text{ MHz}$. Figure 5 shows the input dynamic range of the inverting BP response at V_{o1} output terminal with $R_1 = R_2 = 50 \text{ k}\Omega$ and $C_1 = C_2 = 3.18 \text{ pF}$, which extends up to amplitude of 0.7 V (peak to peak) without signification distortion. The dependence of the output harmonic distortion of BP filter on input voltage amplitude is illustrated in Figure 6. From Figure 6, we can see that the harmonic distortion rapidly increases if the input signal is increased beyond 0.7 V for the chosen DDCC implementation.

5. Conclusion

In this paper, the author also proposes a new high-input impedance voltage-mode multifunction biquadratic filter.

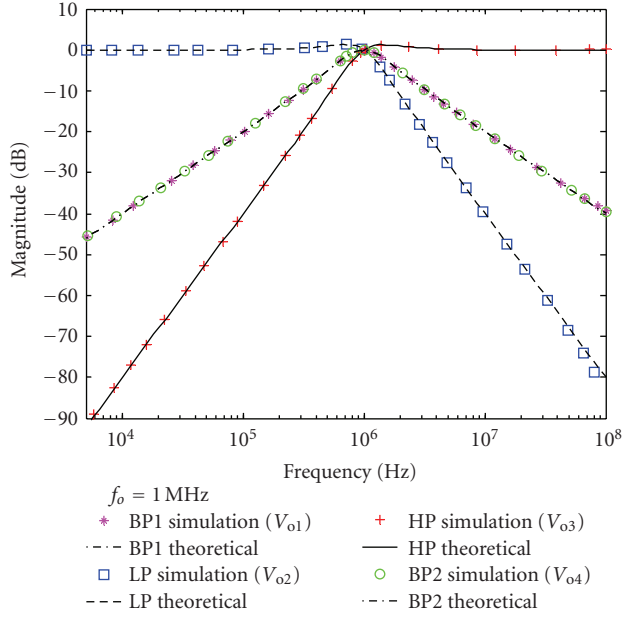


FIGURE 3: Simulated frequency responses of highpass, bandpass, and lowpass of Figure 1 at $f_o = 1$ MHz and $Q = 1$.

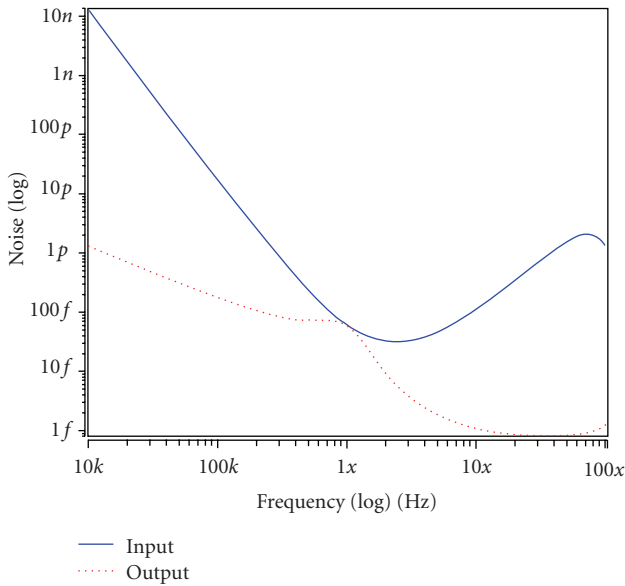


FIGURE 4: Equivalent output and input noise of the bandpass filter versus frequency.

This circuit offers several advantages, such as no requirements for component-matching conditions, the use of only grounded passive components, high-input impedance, and low active and passive sensitivity performances. The proposed circuit has the same advantages reported by [3] which is using two minus-type DDCCs, two grounded capacitors, and two grounded resistors. Moreover, the proposed circuit is simpler in configuration than the old circuit, since the use of only plus-type of DDCCs is simpler than the use of the minus-type of DDCCs. In addition to inverting

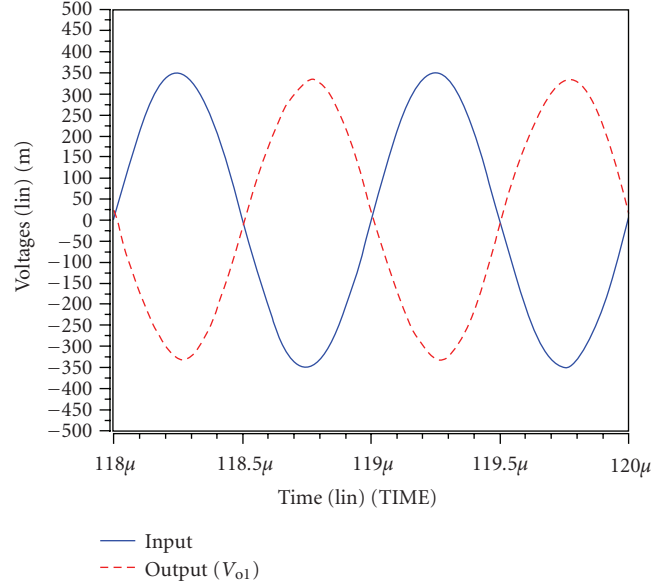


FIGURE 5: The input and output waveforms of inverting BP response for a 1 MHz sinusoidal input of 0.7 V (peak to peak).

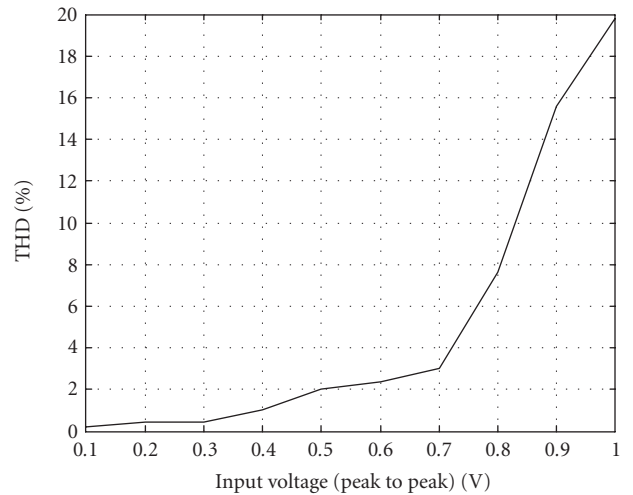


FIGURE 6: THD variations of the BP filter versus amplitudes of the applied sinusoidal voltages at 1 MHz.

highpass, inverting bandpass, and non-inverting lowpass filter responses, the proposed circuit can also realize non-inverting bandpass filter response.

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