

## Research Article

# A New Translinear-Based Dual-Output Square-Rooting Circuit

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A new wide input range square-rooting circuit is presented. The proposed circuit consists of a dual translinear loop, an absolute value circuit, and current mirrors. A current-mode technique is used to provide wide input range with simple circuitry. The output signal of the proposed circuit is the current which is proportional to the square root of input current. The proposed square-rooting circuit was confirmed by using PSpice simulator program. The simulation results demonstrate that the proposed circuit provides the excellent temperature stability with wide input current range.

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## 1. INTRODUCTION

A square-rooting circuit is widely used in analog instrumentation and measurement systems. For example, it is used to linearize a signal from a differential pressure flow meter, or to calculate the root mean square value of an arbitrary waveform [1]. Typically, voltage-mode square-rooting circuits can be realized by using operational amplifiers (op-amps) and can be attached to passive and active elements such as an analog multiplier to form squarer and resistors [2], the BJTs to form a log and antilog amplifier [3], and MOS transistor operating in triode region [4]. However, op-amp-based square-rooting circuit has the high-frequency limitation due to the finite gain bandwidth product (GBW) of the op-amps, and some of them are not suitable for IC implementation. Second-generation current conveyors (CCIIs) are useful in analog signal processing circuits. Since the gain bandwidth product of an op-amp is finite, the higher the gain it realizes, the less bandwidth it possesses. In the past, the realization of square-rooting circuit using CCII has been proposed in the technical literature [5, 6]. Lui [5] proposed square-rooting circuit based on the use of the CCII connected with nonsaturated MOS transistors, op-amps, and resistors. The high-frequency limitation of this circuit is due to the finite GBW of the op-amp and the MOS transistor operated in nonsaturation. Moreover, the use of op-amps and floating resistors makes this circuit not ideal for IC fabrication. Differential difference current conveyors

(DDCCs-) based square-rooting circuit is proposed by Chiu et al. [6]. However, the disadvantage of this circuit is the same as the proposed square-rooting circuits of Lui [5]. The square-rooting circuit is realized by using bipolar junction transistors (BJTs), based on the current-mode technique, which have been reported as being a quite attractive feature of wide bandwidth and suitable for implementing in monolithic form [7]; but only positive input current range can be applied into the circuit. The current-mode square-rooting circuit based on MOS transistors operating in class AB has also been reported [8].

This paper, a new BJT wide input range current-mode square-rooting circuit, is introduced. It consists of a dual translinear loop, an absolute value circuit, and current mirrors. The proposed square-rooting circuit is operated in current mode that has the following advantages.

The square-rooting circuits of Filanovsky and Baltes [4], Liu [5], and Chiu et al. [6] are limited for high frequency due to the finite GBW of op-amps and MOS transistor operated in nonsaturation. While the proposed circuit has no restriction, therefore, the proposed square-rooting circuit operates more high-frequency than that of the previous square-rooting circuits.

- (i) The proposed square rooting is suitable for bipolar IC technology.
- (ii) The proposed square rooting provides wide input current range.

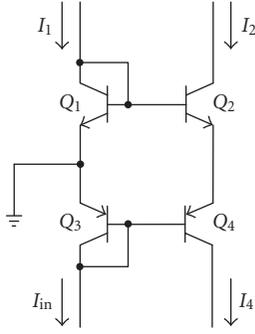


FIGURE 1: Dual translinear loop.

- (iii) The proposed square rooting provides excellent temperature stability.
- (iv) It possesses high output impedance.

## 2. CIRCUIT DESCRIPTION

Figure 1 shows the dual translinear loop of the proposed square-rooting circuit; here  $I_1$ ,  $I_2$ ,  $I_3$ , and  $I_4$  are the currents taken as the collector currents of  $Q_1$ ,  $Q_2$ ,  $Q_3$ , and  $Q_4$ , respectively. Neglect the based currents and assume that the four transistors are identical. Summing the base-emitter voltages around the closed-loop containing  $Q_1$ ,  $Q_2$ ,  $Q_3$ , and  $Q_4$ , gives by [9]

$$V_{be1} + V_{be3} = V_{be2} + V_{be4}. \quad (1)$$

Substituting for the relationship between collector currents  $I_C$  and base voltages  $V_{BE}$  [10] yields

$$\frac{kT}{q} \ln \left( \frac{I_1}{I_S} \right) + \frac{kT}{q} \ln \left( \frac{I_3}{I_S} \right) = \frac{kT}{q} \ln \left( \frac{I_2}{I_S} \right) + \frac{kT}{q} \ln \left( \frac{I_4}{I_S} \right), \quad (2)$$

from which

$$I_1 I_{in} = I_2 I_4. \quad (3)$$

Let  $I_1$  be the constant current source that provides the bias current for the circuit. When the input signal current  $I_{in}$  is applied to the circuit, then the relationship of the currents  $I_2$ ,  $I_4$ , and  $I_{in}$ , since  $I_2$  is equal to  $I_4$ , can be expressed as

$$I_2 = -I_4 = \sqrt{I_1 I_{in}}. \quad (4)$$

It means that the currents  $I_2$  and  $I_4$  are a square root of the input current  $I_{in}$  with the current gain equal to  $\sqrt{I_1}$ . In addition, the temperature effect in terms of the thermal voltage is compensated. It can be noted from Figure 1 that only positive input signal current  $I_{in}$  can be applied to the circuit. To achieve wide input current range that can apply both negative and positive signal currents, the absolute-value circuit is required.

Figure 2 shows the absolute-value circuit. The transistors  $Q_1$ – $Q_4$  and  $I_q$  function as a current-mode full-wave rectifier [11]. The current source  $I_q$  provides the biasing current

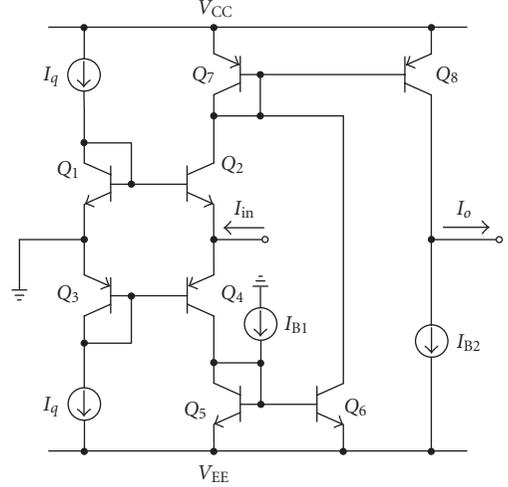


FIGURE 2: Absolute value circuit.

for the circuit. The current mirrors,  $Q_5$ – $Q_6$  and  $Q_7$ – $Q_8$ , are supplied by the current source  $I_{B1}$ , which ensures that the two current mirrors are continuously on, thereby, improving frequency response and linearity overall system. The current source  $I_{B2}$  is used to eliminate the DC current offset of the output current. The output current  $I_o$  of circuit can be expressed as

$$I_o = |I_{in}|. \quad (5)$$

Figure 3 shows the proposed square-rooting circuit using a dual translinear loop, an absolute-value circuit, and current mirrors. In this circuit, the input is a current, and the output is also the dual currents which are proportional to the square root of the input current. Using (4) and (5), the output current can be expressed as

$$I_{out+} = -I_{out-} = \sqrt{I_o} \sqrt{|I_{in}|}. \quad (6)$$

From (6), it means that the output current  $I_{out}$  is a square-root of the input current  $I_{in}$ , with the current gain equal to  $I_o$ . It is also shown in (6) that the output current is not sensitive to temperature. It is noted that the proposed square-rooting circuits in Figure 3 provide the output current which is proportional to the square root of the input current at high output impedance. Hence, it can be directly connected as the load. The proposed circuit in Figure 3 can easily be modified to be as voltage-in current-out or voltage-in voltage-out circuits by using the converting resistances. If the square-rooting circuit with voltage-in current-out circuit is desired, the new input voltage can be applied to the node  $Y$  of absolute-value circuit and disconnect grounded resistor; while its node  $X$  is terminated with grounded resistor. If the square-rooting circuit with voltage-in voltage-out circuit is continually desired, the additional grounded resistor is required to connect at nodes  $Z$  for operating as current-to-voltage conversion.

In the practical realization, the device mismatch between NPN and PNP bipolar transistors groups of  $Q_{11}$ – $Q_{14}$  function is the major factor that contributes to the errors from

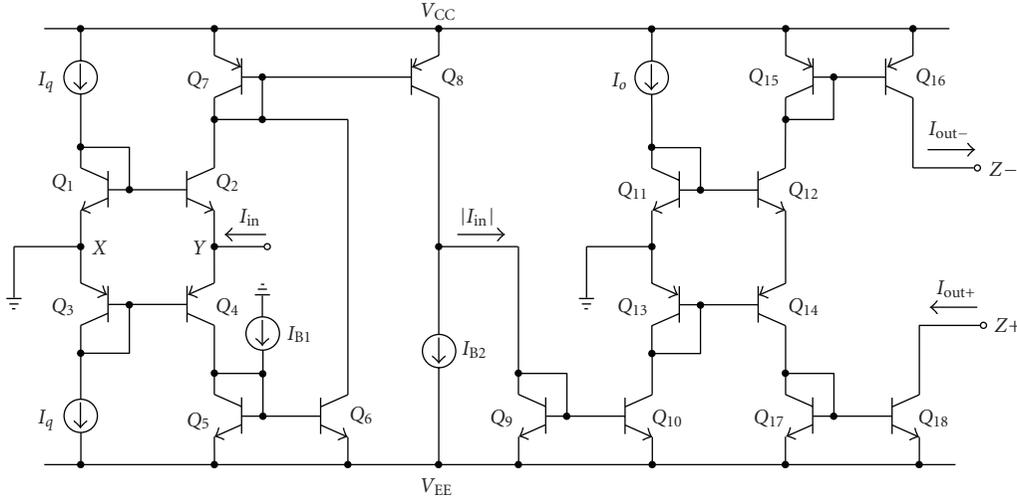


FIGURE 3: Proposed dual-output current-mode square-rooting circuit.

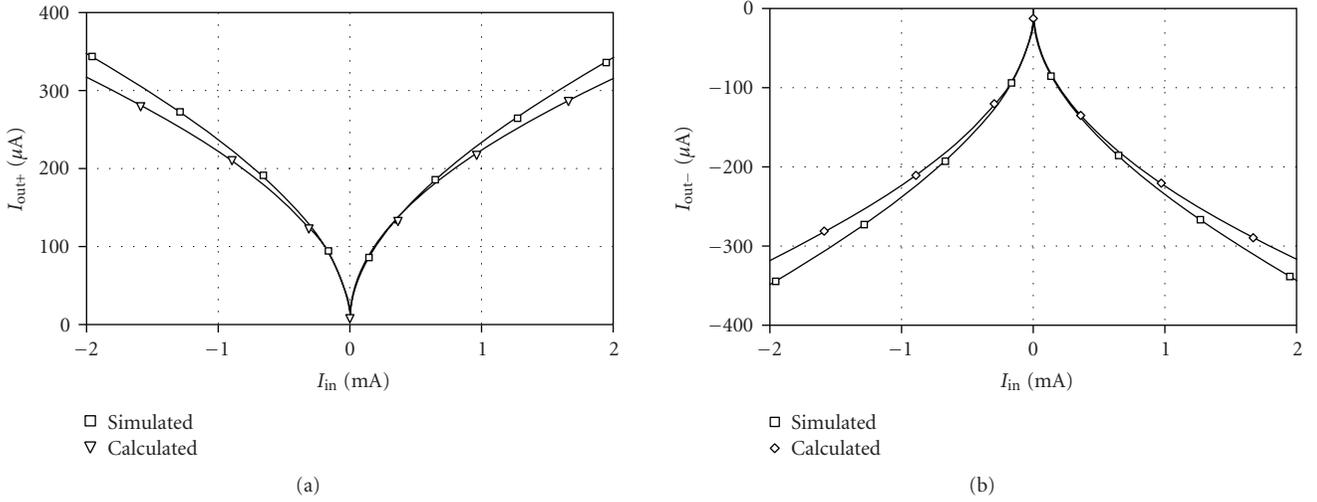


FIGURE 4: Simulated DC transfer characteristics of proposed square-rooting circuit: (a) positive input; (b) negative output.

the ideal performance. The output current error can be expressed as

$$I_{out} = \sqrt{\left(1 - \frac{2}{\beta_N + 2}\right) \left(1 - \frac{2}{\beta_P + 2}\right)} \sqrt{I_o} \sqrt{I_{in}}, \quad (7)$$

where  $\beta_N$  and  $\beta_P$  are the current gains of NPN and PNP bipolar transistors, respectively, and  $I_o$  is the bias current of the circuit. If  $\beta_N = 137.5$ ,  $\beta_P = 110$ ,  $I_o = 50 \mu\text{A}$ , and  $I_{in} = 1 \text{ mA}$ , then the resulting output current error is equal to 2%.

### 3. SIMULATION RESULTS

The square-rooting circuit in Figure 3 is simulated by using the PSpice simulator program. The proposed square-rooting circuit is simulated based on the model parameters of the AT&T ALA400-CBIC-R [12]. The supply voltages are chosen

as  $V_{CC} = 2.5 \text{ V}$  and  $V_{EE} = -2.5 \text{ V}$ . The current supplies are  $I_q = 8 \mu\text{A}$ ,  $I_{B1} = 100 \mu\text{A}$ ,  $I_{B2} = 116 \mu\text{A}$ , and  $I_o = 50 \mu\text{A}$ .

Figure 4 shows the simulated DC transfer characteristic for the input current  $I_{in}$  of the proposed square-rooting circuit in Figure 3. The simulation of transfer curve is compared with the calculated value. This result demonstrates that the proposed square-rooting circuit yields the operating current range from  $< -1 \text{ mA}$  to  $> 1 \text{ mA}$  of the input current. At  $I_{in} = 1 \text{ mA}$  and  $-1 \text{ mA}$ , it also shows that the difference of the output current between simulation value and calculated value is  $10.11 \mu\text{A}$  (4.52%) and  $13.88 \mu\text{A}$  (6.18%), respectively. The amplitude error of the output current signal more than 2% may be resulting from the error of the absolute-value circuit which is neglected.

Figure 5 shows the operation of proposed square-rooting circuit in Figure 3 while applying the  $2 \text{ mA}_{P-P}$  triangle wave with  $100 \text{ kHz}$  frequency at the input. The input and output waveforms are shown in Figures 5(a) and

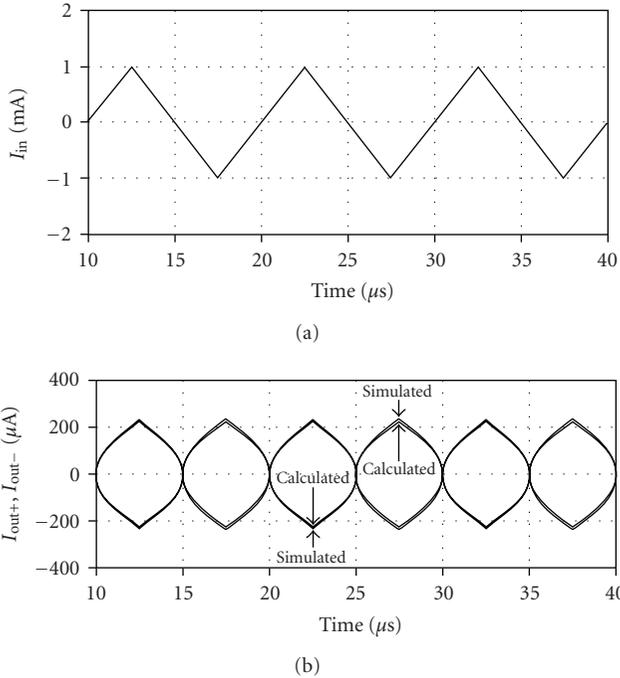


FIGURE 5: Operation of circuit for the 100 kHz input triangular signal: (a) input waveform; (b) output waveforms.

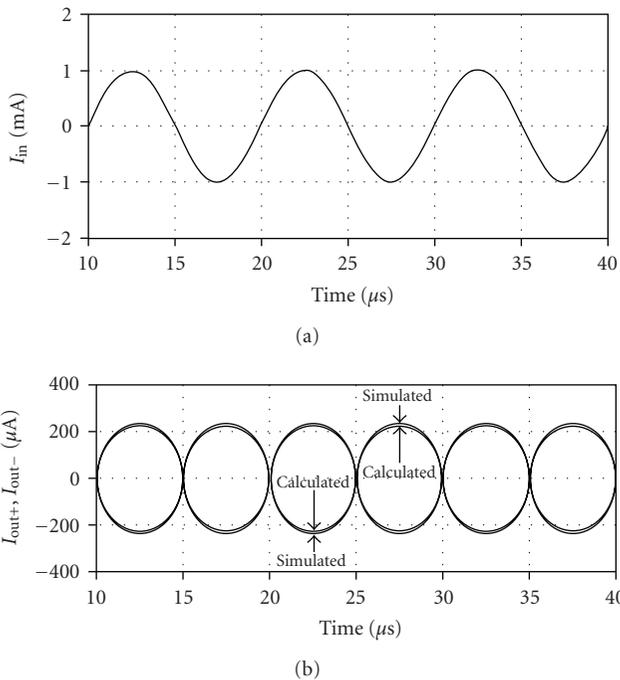


FIGURE 6: Operation of circuit for the 100 kHz sine wave input signal: (a) input waveform; (b) output waveforms.

5(b), respectively. Again, a  $2\text{ mA}_{P-P}$  sinusoidal signal with 100 kHz frequency is applied to the proposed square-rooting circuit in Figure 3. The input and output waveforms are shown in Figures 6(a) and 6(b), respectively. Figure 6 is confirmed while the input is nonlinear, as the output

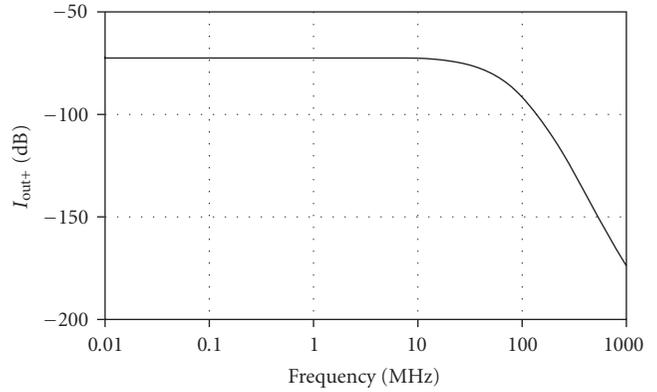


FIGURE 7: Simulated result for frequency responses.

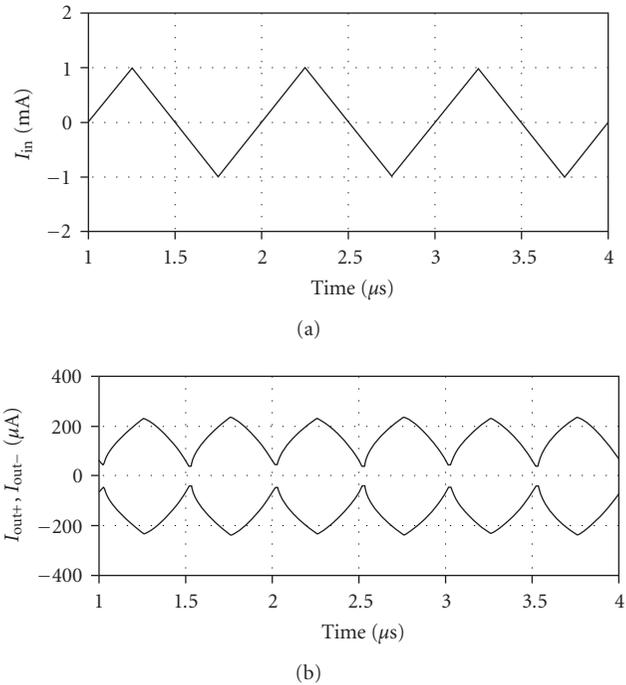


FIGURE 8: Operation of circuit for the 1 MHz input triangular signal: (a) input waveform; (b) output waveform.

corresponds proportionally to the square root for the input. The simulated output waveforms are also compared with the calculated values. The simulated frequency response of the proposed circuits has been done as shown in Figure 7. It should be noted that the bandwidth is about 30 MHz. This simulation, the power consumption, is approximated to 15 mW.

To demonstrate the performance of the proposed square-rooting circuit, Figure 8 shows the simulated output waveform for the cases of the 1 MHz frequency triangle wave input signal and for  $2\text{ mA}_{P-P}$  amplitude. From Figure 8, it is shown that the proposed square-rooting circuit provides the good output waveform at 1 MHz. Figure 9 shows the output current of proposed square-rooting circuit at  $50^\circ\text{C}$ ,  $75^\circ\text{C}$ , and  $100^\circ\text{C}$  temperatures while applying the 100 kHz

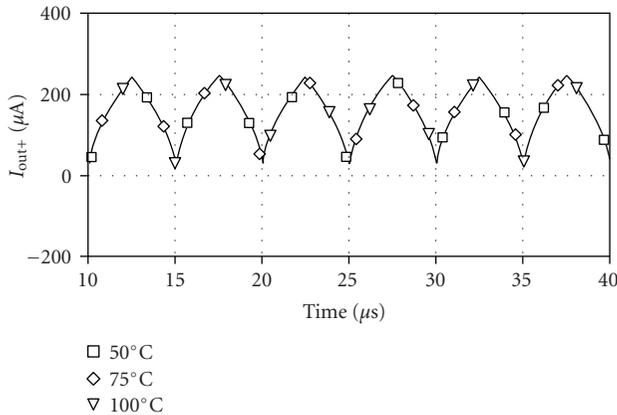


FIGURE 9: Output waveforms at different temperatures at 100 kHz frequency input signal.

frequency triangle wave with  $2\text{ mA}_{P-P}$  amplitude at the input of the circuit. From the simulation result in Figure 9, it is obviously shown that the proposed square-rooting circuit provides the excellent temperature stability; this result can be confirmed as in (6).

#### 4. CONCLUSIONS

In this paper, a new current-mode square-rooting circuit is presented. The proposed circuit employs a dual translinear loop, an absolute-value circuit, and current mirrors. Simulation results show that the proposed square-rooting circuit provides the wide input current range with excellent temperature stability. Better performance can be expected by using the bipolar transistors and the parameters of complementary high performance processes which were not available to the authors. The proposed square-rooting circuit is suitable for IC fabrication because of the absence of the external resistor.

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