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NOVEL FIRST-ORDER CURRENT-MODE ALL-PASS SECTIONS USING CCIII

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Two new configurations realizing canonical first-order current-mode all-pass sections (APSs) using a single third generation current conveyor (CCIII) are given. Using each configuration, two types of first-order all-pass filters can be derived giving rise to four distinct circuits for APS, three of which are novel. Each APS employs only a single CCIII and a minimum of passive components: one resistor and one capacitor. The circuits are suited for MOS implementation. The SPICE simulation results for frequency response as well as transient response are incorporated to verify the theory.

Keywords: Current conveyors; All-pass filters

1 INTRODUCTION

Current conveyors have become very popular as these devices provide high performance and greater functional versatility in realizations [1]. Several first-order voltage-mode all-pass sections (APSs) using current conveyors are available in technical literature [2–4]. However, current-mode (CM) circuits are also receiving much attention for their potential advantages such as inherent wider bandwidth, simple circuitry, lower power consumption, and wide dynamic range [5]. Considering these advantages of CM circuits, several CM-APSs using different active devices have been reported but many of them use large component count or matching conditions [6–8].

Recently, a third generation current conveyor (CCIII) introduced by Fabre (1995) was used in realizing first-order voltage-mode and a canonical CM-APS [9, 10]. In this paper, two configurations for first-order CM all-pass filters are proposed. Each configuration uses a single active element (CCIII) and two passive components, does not require any matching condition, and results in canonical structures [11]. Two different types of APSs can be derived from each configuration by appropriate choice of two passive components thus giving rise to four distinct circuits for APS, three of which are novel and one is available in literature [10]. All the circuits possess attractive sensitivity features, low component count, and are suited for MOS implementation as the resistor can be conveniently implemented in MOS technology. Simulation results are included to verify the theory.

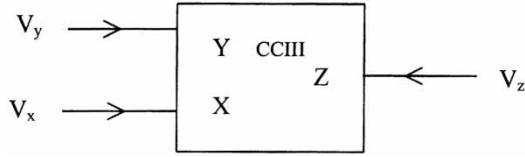* Corresponding author. E-mail: maheshwarispm@rediffmail.com

FIGURE 1   A third generation current conveyor symbol.
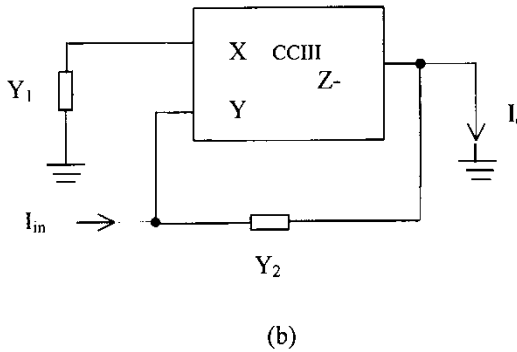
2   THE CIRCUITS

The CCIII symbol is shown in Figure 1 and is characterized by the following relationship.

$$i_y = -i_x, \quad V_x = V_y, \quad i_z = pi_x \tag{1}$$

where $p = 1$ for CCIII+ and $p = -1$ for CCIII− [10]. The proposed first-order CM-APS configurations are shown in Figure 2. Each configuration uses only a single CCIII, one resistor,
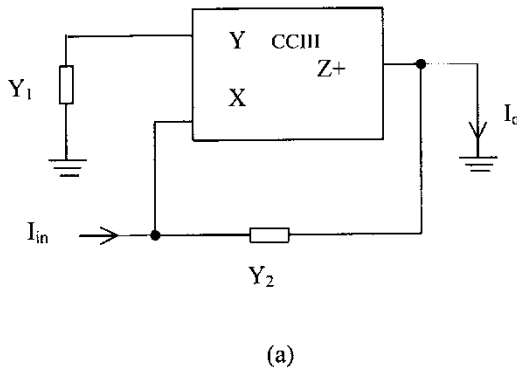
(a)

(b)

FIGURE 2   (a) All-pass filter configuration using a CCIII+; (b) all-pass filter configuration using a CCIII−.

and a capacitor and results in a canonical structure. The generalized current transfer function for the two configurations is analyzed as:

$$\frac{I_o}{I_{in}} = \frac{Y_2 - Y_1}{Y_2 + Y_1}. \tag{2}$$

Obviously, this form of transfer function given in Eq. (2) is suitable for first-order all-pass realization. Using each of the two proposed configurations, a designer can derive two different current transfer functions by choosing Y_1 and Y_2 appropriately as given below.
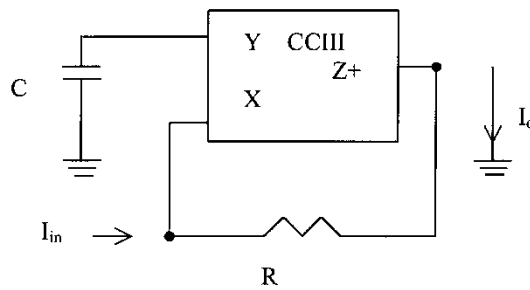
Choice 1: $Y_1 = sC$ and $Y_2 = 1/R$ yields

$$\frac{I_o}{I_{in}} = -\frac{s - (1/RC)}{s + (1/RC)}. \tag{3}$$
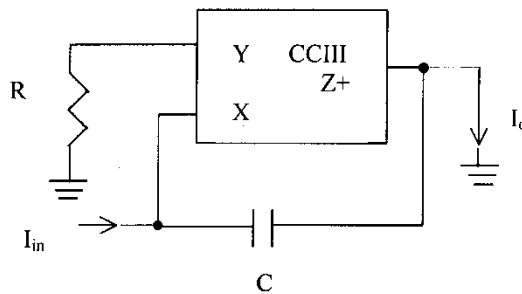
Choice 2: $Y_1 = 1/R$ and $Y_2 = sC$ yields

$$\frac{I_o}{I_{in}} = \frac{s - (1/RC)}{s + (1/RC)}. \tag{4}$$

It is evident that the choice 1 gives an APS with a phase shift from 0 to $-\Pi$ and choice 2 gives an APS with a phase shift from Π to 0. The configuration of Figure 2a with choice 1
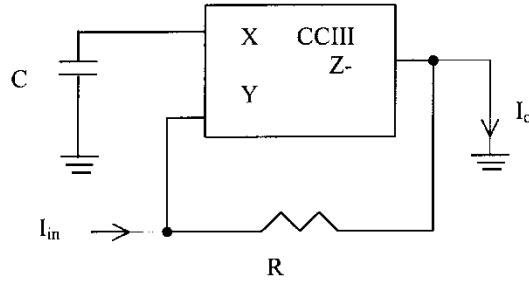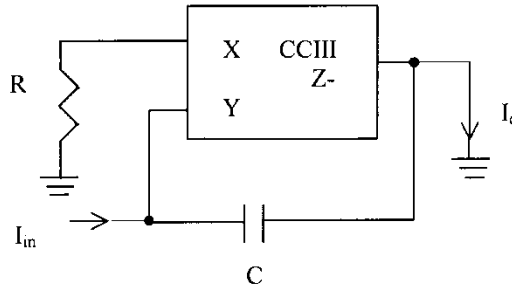

(a)

(b)

FIGURE 3   (a) CM-APS-I; (b) CM-APS-II.

(a)

(b)

FIGURE 4   (a) CM-APS-III; (b) CM-APS-IV.

gives APS-I and with choice 2 gives APS-II. Figures 3a and b show APS-I and APS-II, respectively. Similarly, the configuration of Figure 2b with choice 1 gives APS-III and with choice 2 gives APS-IV. Figures 4a and b show APS-III and APS-IV, respectively. It is to be noted that of the four APSs, the first three (APS-I, II, and III) are new, however, the circuit of APS-IV is available in literature where it was derived from the voltage-mode APS [10].

3   ACTIVE AND PASSIVE SENSITIVITIES

Taking into account the non-idealities of CCIII, Eq. (1) can be modified as:

$$i_y = -\gamma i_x, \quad V_x = \alpha V_y, \quad i_z = (p\beta)i_x \tag{5}$$

where $\gamma = (1 - k_1)$, $\alpha = (1 - k_2)$, $\beta = (1 - k_3)$, k_1 and k_3 are current transfer errors and k_2 is the voltage transfer error. Using Eq. (5), the three new circuits of Figures 3a, b and 4a are analyzed and the non-ideal current transfer functions are found as:

$$\text{APS-I:} \ \frac{I_o}{I_{in}} = -\beta \frac{s - (\alpha\gamma/\beta)(1/RC)}{s + (\alpha\gamma)(1/RC)}. \tag{6}$$

TABLE I Sensitivity Figures for the Proposed APSs.

Circuit	$S_\alpha^{\omega_o}$	$S_\gamma^{\omega_o}$	$S_\beta^{\omega_o}$	$S_{R,C}^{\omega_o}$	S_α^{H}	S_γ^{H}	S_β^{H}	$S_{R,C}^{H}$
APS-I	1	1	0	−1	0	0	1	0
APS-II	−1	−1	0	−1	0	0	0	0
APS-III	−1	−1	0	−1	0	−1	1	0

$$\text{APS-II:} \quad \frac{I_o}{I_{in}} = \frac{s - (\beta/\alpha\gamma)(1/RC)}{s + (1/\alpha\gamma)(1/RC)}. \tag{7}$$

$$\text{APS-III:} \quad \frac{I_o}{I_{in}} = -\left(\frac{\beta}{\gamma}\right)\frac{s - (1/\alpha\beta)(1/RC)}{s + (1/\alpha\gamma)(1/RC)}. \tag{8}$$

The incremental sensitivities of pole (ω_o) and gain (H) to active and passive components are analyzed for the three APSs described by Eqs. (6)–(8) and given in Table I. It is evident from the sensitivity table that the pole (ω_o) and gain sensitivities to the active and passive components are within unity in magnitude. Thus, the three new APS circuits enjoy attractive active and passive sensitivity performance.

4 SIMULATION RESULTS

The proposed CM-APSs were verified using SPICE simulations. The CMOS implementation of CCIII was used in simulation with ± 5 V supply and $2\,\mu$m CMOS parameters [12]. The circuit of Figure 3a (APS-I) was designed for a $-90°$ phase-shift at 100 kHz. The designed values were as $C = 1$ nF and $R = 1.59$ K. The simulated results for the frequency response are given in Figure 5. Similarly, a phase shifter was designed using the APS-II of Figure 3b for a $90°$ phase-shift at 100 kHz. The designed values of components were as above and the results for the frequency response are shown in Figure 6. The results for the frequency response of the proposed circuits are in agreement with the theory.
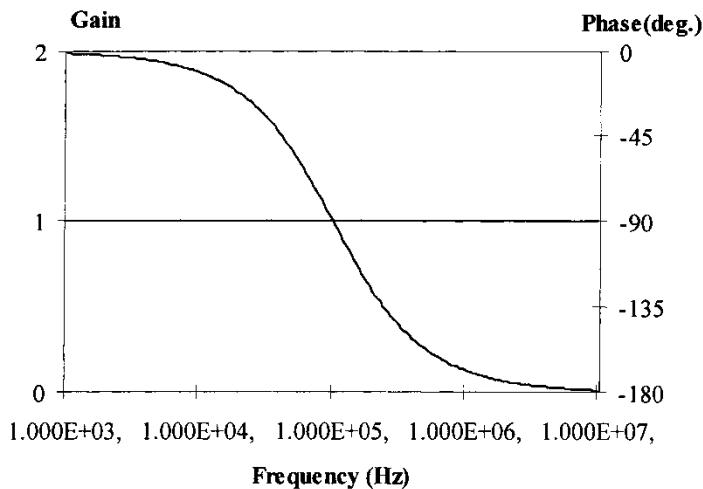

FIGURE 5 Simulated frequency response for APS-I.

Gain   **Phase (deg.)**
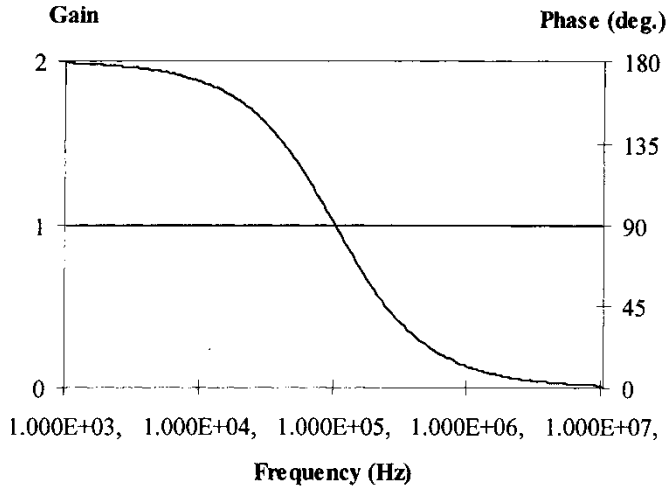

FIGURE 6   Simulated frequency response for APS-II.

Next, the transient response of APS-II designed as a phase shifter was studied. The designed values were as $C = 1\,nF$ and $R = 1.59\,K$. A sinusoidal current input of 0.1 mA peak at 100 kHz was applied and the output current obtained with the desired phase-shift of 90°. The results for the transient response are shown in Figure 7. The THD results for the APS-II with the above designed values are also given in Figure 8 and show that the low-level input currents of amplitude till $110\,\mu A$ ($220\,\mu A$ peak to peak) results in THD values less than 1%. Thus, the transient response and low THD results confirm the practical utility of the proposed circuits.
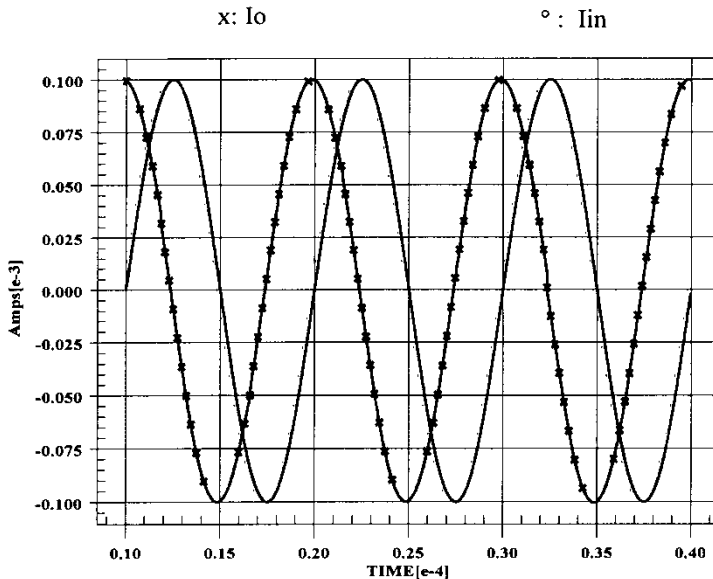
x: Io   °: **Iin**

FIGURE 7   Time-domain waveforms of the APS-II for input frequency 100 kHz.
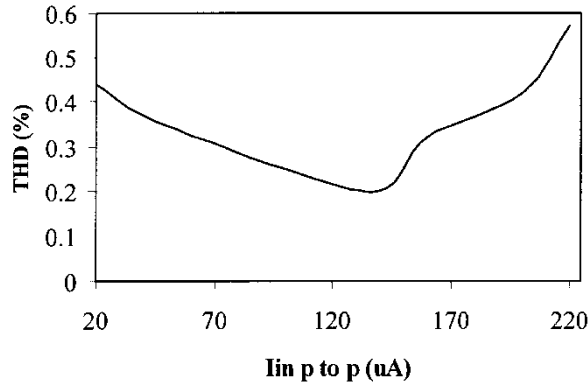
FIGURE 8 THD results for APS-II with 100 kHz sinusoidal input.

5 CONCLUSION

Two new configurations for CM first-order all-pass sections using a single CCIII are introduced giving rise to four distinct circuits, three of which are novel. The circuits are suited for MOS implementation. The proposed configurations are canonical, require no matching constraints, realize two types of all-pass filters, possess low active and passive sensitivities, low THD, and are verified by attractive simulation results.

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