Active and Passive Elec. Comp., September 2003, Vol. 26, pp. 151–166

ULTRA-LOW TEMPERATURE COEFFICIENT OF CAPACITANCE (TCC) OF THE $SrSnO_3$-BASED ELECTRICAL COMPONENTS

ABDUL-MAJEED AZAD[a,*], TOH YEN PANG[b] and MOHAMMAD A. ALIM[c,†]

[a]NexTech Materials, Ltd., 720-I Lakeview Plaza Boulevard, Worthington, OH 43085, USA;
[b]Department of Aerospace Engineering, RMIT, Melbourne 3001, Victoria, Australia;
[c]Department of Electrical Engineering, Alabama A & M University, P.O. Box 297, Normal, Alabama 35762, USA

(Received 23 September 2002; In final form 17 November 2002)

The perovskite-structured $SrSnO_3$ possessing steady capacitance over the temperature range between 27 °C and 300 °C in a frequency domain spanning nearly four decades has been evaluated. The samples investigated in this study were synthesized by using solid-state reaction (SSR) and self-heat-sustained (SHS) techniques. These samples were sintered at a temperature (T) ranging between 1200 °C and 1600 °C with a soak-time (t) ranging between 2 h and 60 h. The ac immittance (impedance or admittance) measurements were conducted on these sintered bodies in the frequency range 5 Hz to 13 MHz. These ac electrical data were found to exhibit relaxation in more than one complex plane formalisms in a simultaneous manner. The magnitude of the terminal capacitance was found to be in a narrow window of 3 pF to 6 pF possessing very weak temperature dependence. Further analysis also revealed that this material system possessed low dielectric constant and ultra-low temperature coefficient of capacitance (TCC) or dielectric constant (TCK). The electrical behavior of these sintered bodies has been systematically correlated with the evolved microstructures. Plausible equivalent circuit elements were extracted using the lumped parameter/complex plane analysis (LP/CPA) and evaluated at various situations.

Keywords: Strontium metastannate; Capacitor component; Electroceramics; Dielectrics; Complex plane analysis; Temperature coefficient of capacitance; Temperature coefficient of dielectric constant; Microstructure-property correlation

1 INTRODUCTION

The perovskite-structured compounds in the $MO–SnO_2$ (M = Ca, Sr, and Ba) system, represented as $MSnO_3$, have been projected as novel electroceramic material due to their potential applications as novel gas sensors and capacitor components in a variety of electronic circuits. The temperature coefficient of capacitance (TCC) or dielectric constant (TCK) becomes an important parameter in the R–C (resistance–capacitance), R–L (resistance–inductance), R–L–C (resistance–inductance–capacitance) or hybrid circuit elements as high dielectric loss results in the generation of heat during the operating processes at normal operating

* E-mail: azad@nextechmaterials.com
† Corresponding author. E-mail: malim@aamu.edu

ISSN 0882-7516 print; ISSN 1563-5031 online
DOI: 10.1080/1042015031000073814

conditions. These operating conditions include fluctuations in the applied voltages, currents, frequencies, temperatures, etc. This generation of heat causes the increase in temperature of the capacitors, which in turn makes the functioning of the associated components complicated. In such applications, the required level of variation with temperature ideally should either be zero or a small reproducible value (negative-positive zero, NP-0) that compensates for a variation in the rest of the circuit [1].

As the improved technologies are emerging in the areas of computers and communications, the electronic information is also progressing in a large volume. Therefore, the demand for equipment with accurate and quick information dissemination is growing. To meet these demands, electronic devices must use higher frequencies than ever before. The non-variance of capacitance or dielectric constant with frequency in the MHz to GHz regime makes the components attractive as a microchip component in the telecommunications, microwaves, and radio applications [2]. It is, thus, imperative that investigations be carried out on material systems that conform to these requirements.

The details of synthesis, processing and microstructural evolution in the $MSnO_3$ compounds have recently been reported [3–5]. With an aim to exploit these materials as electrical components on a commercial scale, possessing the aforementioned temperature and frequency-independent characteristics, a thorough understanding of the nature of the electrical conduction in these materials is warranted. As these devices are made mostly from the polycrystalline material system, it is important to understand the effect of microstructural variation and the sequential contribution of grains, grain-boundaries, and other phases including relevant physically distinct regions in the microstructure.

The a.c. small-signal electrical characterization of the sintered calcium metastannate ($CaSnO_3$), using the lumped parameter/complex plane analysis (LP/CPA) technique, has recently been reported [6–8]. In these reports, it was amply demonstrated that $CaSnO_3$ is a potential candidate for application in several types of electronic devices and appliances as a low K (capacitance or relative dielectric constant), high resistance, and low TCC-TCK material between room temperature and up to 300 °C in the frequency range between 1 kHz and 10 MHz.

In this paper, similar measurements and analyses on the Sr-based $MO–SnO_2$ analogue (such as $SrSnO_3$) are reported. The as-acquired electrical data in the immittance (impedance or admittance) form for this material system at the temperature (T) range above room temperature through 300 °C, in conjunction with the applied frequency (f) ranging between 5 Hz and 13 MHz, have been analyzed. The results on the extracted capacitance or dielectric constant including the loss tangent ($\tan\delta$) as a function of elevated temperature and applied frequency are presented.

2 EXPERIMENTAL

The samples investigated in this work were synthesized via two techniques, viz., the traditional solid-state reaction (SSR) route, and a novel method called the self-heat-sustained (SHS) route. Details of the preparative and characterization techniques have been reported elsewhere [5]. It should be pointed out that the idea of adopting various synthesis processes was two-fold. First, the limited amount of literature involving the SSR route available on this material is presumed to be a conventional method. Second, it was intended to find a favorable synthesis technique in terms of the phase purity and benign microstructure in the sintered samples with desired electrical characteristics.

The a.c. electrical data for these sintered samples were acquired over a wide range of applied frequencies ($5\,\text{Hz} < f < 13\,\text{MHz}$) using the HP4192A LF Impedance Analyzer

(Hewlett-Packard, Yokogawa, Japan). The data acquisition was accomplished using a fully automated experimental control via a desktop personal computer as the instrument controller. The small-signal amplitude was about 1 V and the acquired a.c. data were reproducible with the varying signal voltage amplitude. These data were analyzed using a proprietary software package [9]. This package allowed automated data acquisition in any of the desired forms such as impedance or admittance or phasor, including analyses in the four complex plane formalisms and Bode plane analysis [10–12]. Necessary electrical parameters were extracted from these representations of the a.c. electrical data that employed complex non-linear least-squared (CNLS) curve-fitting procedure [9–12]. This extraction procedure does not assume or simulate any equivalent circuit configuration a priori, which is often done using commercial software.

Small slices of sintered samples were coated with silver paint (Electrolube Ltd., UK), cured at 500 °C for 2 h, and secured between two highly polished circular stainless steel discs (mounted on Perspex walls) serving as electrodes. The sliced sample was fitted with adjustable screws on both sides of the holder. This arrangement allowed better sample-holding capability in the accessories for the HP4192A at room temperature. The stainless steel screws serving as contact electrodes with the silver paint did not exhibit any contribution to the terminal immittance as it formed an ohmic contact (resistance $\leq 2\,\Omega$). For the acquisition of the a.c. data at elevated temperatures (above room temperature through 300 °C), an indigenously designed and fabricated stainless steel sample holder was mounted on an alumina brick ($25\times25\times10\,mm^3$). To ensure good adherence, high-temperature alumina cement was used and cured at 225 °C for 30 min. Gold wires, 0.25 mm in diameter (D.F. Goldsmith Chemical and Metal Corp., Evanston, Ill, USA) were used as electrode leads. Each sample was introduced into the uniform temperature zone of a custom-designed small, low-thermal mass, precalibrated horizontal furnace. The furnace was heated to the desired temperature; at a constant rate of 10 °C/min. Sufficient time was allowed to equilibrate at the measurement temperature within the sample before the acquisition of a.c. electrical data. The temperature fluctuations at the measurement points were not more than ±1 °C. The sample thickness and the electrode area in all the measurements were kept identical so that the geometric configuration ensures a fixed effect to the terminal immittance data. Thus, the terminal immittance data did not require a state of normalization [10–12] for the entire analysis. As an example, it can be mentioned that the terminal capacitance can be converted to the relative dielectric constant using the state of normalization [10–12].

3 RESULTS AND DISCUSSION

The detailed analyses of the a.c. electrical data have been performed for all the samples fabricated utilizing T–t (temperature and soak-time) profiles via the SSR or SHS route. These data were acquired as a function of the ambient temperature ranging between 27 °C and 300 °C. Thus, the analytical representation involved four complex plane formalisms [10–12], Bode plane analysis, variation of the terminal capacitance and relative dielectric constant selected arbitrarily at any measurement frequency.

In general, semicircular relaxation(s) may be expected in any of the complex plane formalisms. The entire samples investigated revealed semicircular relaxation(s) in the impedance (Z*), complex capacitance (C*), and modulus (M*) planes. There was no meaningful feature of the as-acquired data in the admittance (Y*) plane. The general features of the a.c. data included:

(a) single-like (i.e., single) semicircular relaxation in the Z*-plane,

(b) a semicircle at the high-frequency region including a vertical line parallel to the imaginary (y-) axis at the low-frequency region in the C*-plane,
(c) mostly a single-like but in some cases overlapped (like-two) semicircle in the M*-plane (for the purpose of clarity, the discussion has been divided into two subsections according to the method adopted for the raw powder synthesis), and
(d) often display of the flat line parallel to the temperature- or frequency-axis (x-axis) for capacitance or relative dielectric constant.

3.1 Electrical Behavior of the SSR-derived $SrSnO_3$

As an example of the analyses of the a.c. electrical data, Figure 1 is selected. It represents room temperature (27 °C) complex plane plots for SSR derived $SrSnO_3$ samples, sintered at 1200 °C with 24 h soak-time. Figure 1a is the total behavior in the Z*-plane. The same data are displayed the C*-plane in Figure 1b. The two distinct relaxations in the M*-plane are depicted in Figure 1c. Figure 1a reveals the lumped total resistance R_{total} $(=R_g + R_{gb})$ in terms of the length of the chord on the real (x-) axis and gives a value of 40.6 MΩ. The lumped capacitance extracted from the peak-frequency ($f_p = \omega_p/2\pi$, $\omega_p R_s C_s = 1$, $\omega = 1/\tau$, where τ is the time constant or the relaxation time) was found to be about 7 pF $(=C_{total})$. The peak-frequency is defined as the frequency corresponding to the highest peak of the semicircular relaxation [10–16]. Fitting of the low-frequency semicircular relaxation in the M*-plane (Fig. 1c) yielded a value of C_{gb} to be about 3.1 pF. The peak-frequency of this relaxation yielded about 23.1 MΩ. This is designated as the grain-boundary resistance, R_{gb}. Combining the two resistance values, the grain resistance, R_g $(=R_{total} - R_{gb})$ could be derived as 17.5 MΩ. The fitting of the high-frequency semicircle in the M*-plane likewise yielded a value of C_g to be 7.5 pF.

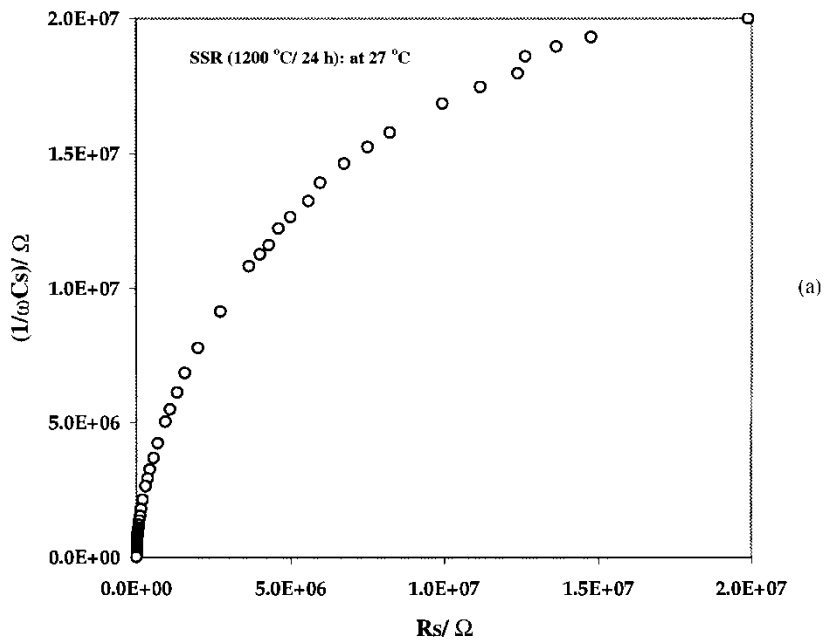


FIGURE 1 Room temperature complex plane plots for the $SrSnO_3$ samples synthesized via SSR and sintered at 1200 °C with soak-time 24 h. (a) Impedance (Z*) plot, (b) complex capacitance plot (C*) plot of the same data as in (a), (c) modulus (M*) plot of the same data as in (a).

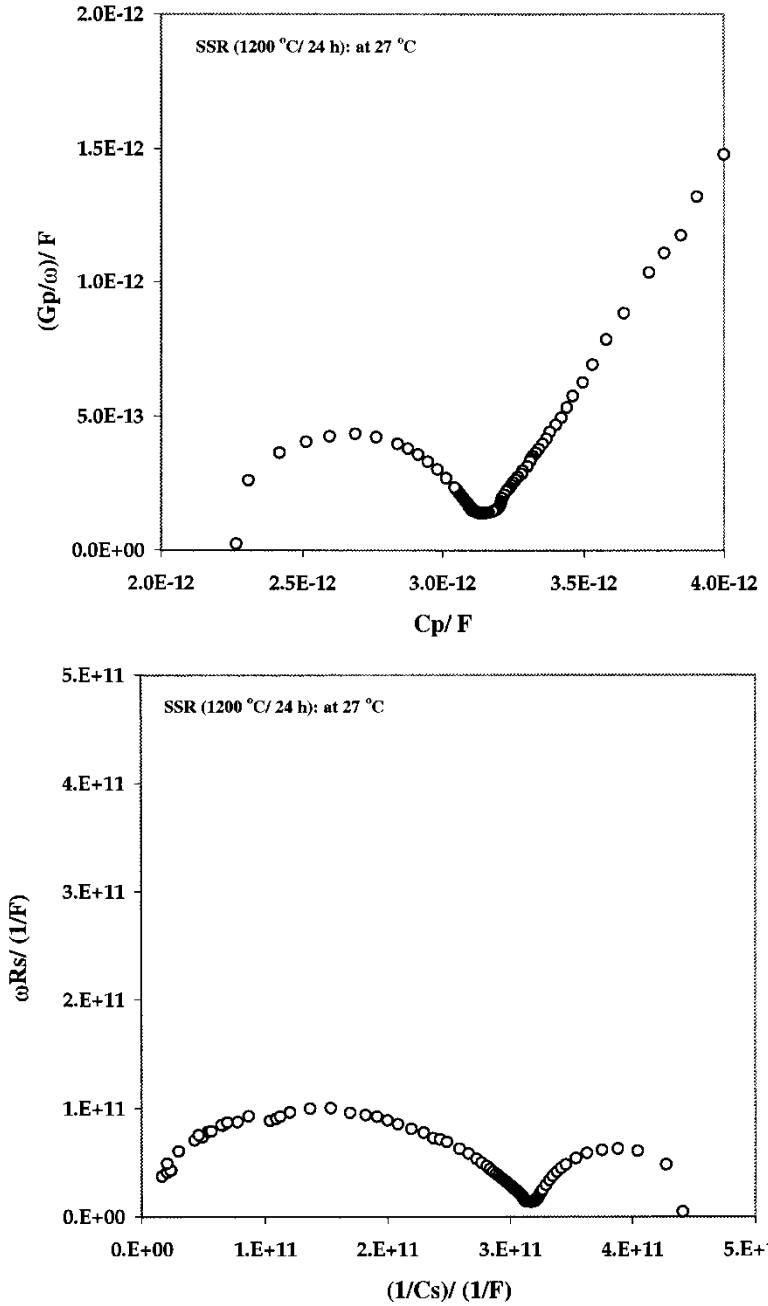


FIGURE 1 (Continued)

When the LP/CPA technique was applied to the same data in the C*-plane (Fig. 1b), the finite left-intercept (C_2) on the real (x-) axis was found to be 2.2 pF. A finite intercept on the left-side of the semicircular relaxation in a complex plane formalism is known as the left-intercept [10–13, 16]. The semicircular relaxation between the high-frequency terminal and the low-frequency asymptotic segment yielded the capacitance ($C_2 + C_1$) to be about 3.1 pF. This gave a value of 0.9 pF for C_1 and 7.6 pF for the terminal capacitance

($C_{total} \sim C_{\infty}$ as $f \to 0$). Since this extraction provides an approximation, it is reasonable to note that this is close to what is obtained in the Z*-plane. The terminal admittance at ultra-low frequencies (i.e., near dc limit) appears to be dominated by the dc conductance in the C*-plane. The minute difference for C_2 (=C_g) and C_{total} obtained from the Z*- and C*-planes is attributed to the reasonable error limit within the CNLS curve-fitting technique. The parameter C_1 is the trapping capacitance, which is a series event with the corresponding resistance R_1 due to the trapping and de-trapping effect. Such a trapping response was also observed in the ZnO-based varistor materials [13–16], and the same explanation applies here as well. The trapping capacitance, however, is not treated the same way as is done in ZnO-based varistors [13, 14] because of its less sensitivity as well as complexity as a function of the ambient temperature.

The left-intercept on the real axis (x-axis) of the C*-plane represents a lumped capacitance response of the barrier layer effect originated at the grain-boundary regions in conjunction with the single crystal-like behavior of the grain. However, a comparison of the relative magnitudes of the lumped grain and grain-boundary capacitance indicates that the contribution of the lumped grains constituting C_2 is likely to be small compared to the barrier layer effect at the grain-boundaries. Thus, the geometric capacitance associated with the barrier layer is the dominating component within C_2, and hence can be referred to as the barrier layer capacitance. The capacitance C_2 is predominantly dictated by a trap-free electrical thickness across the grain-boundaries, which sustains a major portion of the applied electrical field under a non-equilibrium condition. The electrical field drop across the lumped grains is much smaller than the electrical field across the lumped grain-boundary electrical length. This is due to the large dc conductivity and is attributed to the donors within the lumped grains. The electrical length, therefore, applies to the physical regions that allow sustaining of the applied voltage due to its high resistance. Such an electrical length can alternately be termed as either electrical thickness or electrical thinness depending on the context for the same physical region across the grain-boundaries. The bulk dielectric behavior of the lumped grains mentioned earlier is, thus, incorporated into C_2. This bulk property can be isolated at ultra-high frequencies (in this case exceeding 13 MHz), exhibiting a lead-electrode related post-inductive response. However, this is not done here due to the limitation of the instrument. The post-inductive response at high frequencies, exceeding 13 MHz, is displayed in reference [17] for ZnO varistors.

The C*-plane relaxation does not give the grain bulk resistance (R_g); it can only give C_g. Likewise, the grain boundary resistance (R_{gb}) in the C*-plane is masked under R_{dc} (or R_{total}) in the Z*-plane. This shows that grain and grain-boundary resistances are different from each other, otherwise dual relaxation in the C*- as well as in the Z*-plane would not have been observed. This is exactly the case, as the aforementioned analyses of the a.c. data in the two complex planes have demonstrated. It is worthwhile to note that the nature of the complex plane representation for other samples sintered at other profiles exhibited identical features as provided in Figure 1. However, the sample resistance continues to be high although the measurements were carried out at elevated temperatures. Usually this behavior is recognized by the nature of the impedance plane where the data below 5 Hz were not available to demonstrate the completeness of the semicircular behavior. Nevertheless, the entire data reveals that a relaxation is highly pronounced which is fitted for understanding material system.

The as-measured electrical parameters (for example: admittance consisting of the parameters C_p and G_p as a function of frequency) of the sample were used to obtain terminal capacitance ($C = C_p$) and relative dielectric constant ($k = C\,(d/A)/\varepsilon_0$, where d is the thickness of the sample, A the cross-sectional area, and ε_0 the permittivity of the vacuum being equal to $8.854 \times 10^{-12}\,F\,m^{-1}$) as a function of frequency. A representative plot of capacitance versus

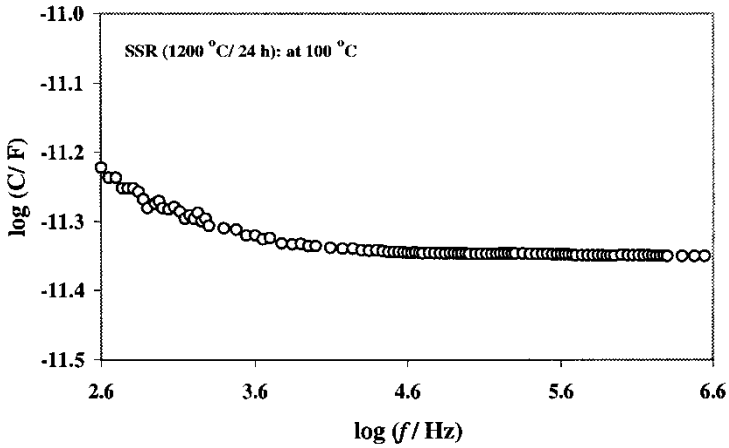


FIGURE 2 Frequency dependence of the terminal capacitance at 100 °C for the sample sintered at 1200 °C with 24 h soak-time.

frequency measured at 100 °C is provided in Figure 2. The capacitance (and the derived relative dielectric constant) remained flat over a wide range of frequency. This domain is estimated to be over 3 decades in the measurement frequency. A very small value of capacitance (a few pF) and a reasonable value of the relative dielectric constant (average value ∼6.5) were monitored for these samples. The slight upward trend seen in the low-frequency domain indicated possible polarization effect at the interfaces consisting of the two opposite electrodes onto the surfaces across the sample. Overall, the invariant nature of these parameters is maintained at higher measurement temperatures. The weak temperature dependence of the derived relative dielectric constant can be observed in Figure 3. Also a value of ∼5 pF could be assigned to the sample capacitance over the measurement temperature range 27 °C through 300 °C. Such a behavior is nearly independent of soak-time. Thus, the capacitance of $SrSnO_3$ possesses not only weak temperature dependence but also remains very steady over a wide range of measurement frequency encompassing almost 4 decades. Average values of these parameters were computed from the linear region of the capacitance versus frequency plots for every sample with different thermal history at various measurement temperatures.

In order to assess the magnitude of the temperature coefficient of capacitance (TCC) and that of the relative dielectric constant (TCK), the values were fitted into a simple linear

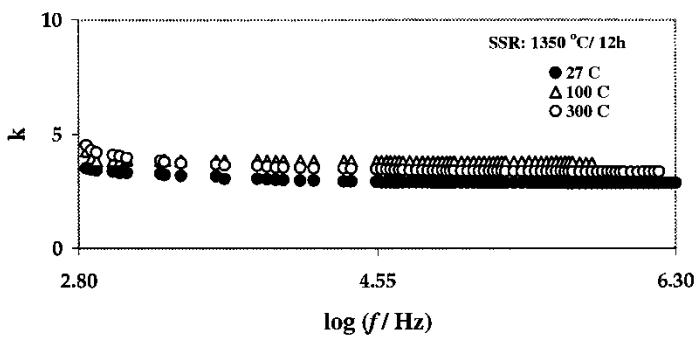


FIGURE 3 Temperature dependence of the relative dielectric constant as a function of applied frequency for the $SrSnO_3$ samples sintered at 1350 °C with soak-time 24 h.

equation of the form, $y = mx + c$, as a function of elevated temperature (here m is the slope of the straight line). The variation of the terminal capacitance with temperature is shown in Figure 4. The values of this parameter were chosen from the flat region of the response (such as the information provided in Fig. 2). The very weak temperature dependence of the terminal capacitance (and the relative dielectric constant) can readily be assessed from the very small value of the slope (of the order of ppm per °K). The TCC and TCK of a dielectric are defined by the relations $TCC = (1/C)(\partial C/\partial T)$, and $TCK = (1/K)(\partial K/\partial T)$. The parametric equations describing the linearity of the values in Figure 4 are listed in Table I in conjunction with the values of TCC and TCK computed in each case.

A representation of the microstructural evolution for the SSR-derived samples sintered at 1200 °C is shown in Figure 5. The morphological features consist predominantly of agglomerates and look identical; except for slight densification as the soak-time increases [5]. This might explain the only minor difference in the terminal capacitance and the dielectric behavior of the $SrSnO_3$ samples.

In an earlier investigation [5], it was found that the sintering at 1350 °C with a hold-time ranging between 12 h and 24 h was most suitable for the dense microstructure development in the solid-state derived samples. The effect of varying sintering schedule on the microstructure result in nearly identical behavior of the $SrSnO_3$ samples as evaluated via the conventional Bode plots as a function of elevated temperature.

3.2 Electrical Response of the SHS-derived $SrSnO_3$

The dispersion of the a.c. electrical data with the applied frequency is displayed in Figure 6. It represents the utilization of the three complex planes (such as Z*-, C*-, and M*-) for the SHS-derived $SrSnO_3$ sample sintered at 1350 °C with 2 h soak-time. The impedance plot depicted in Figure 6a represents the data acquired at 100 °C while Figures 6b and 6c represent the data acquired at 27 °C. The sample exhibits a very high resistance (several MΩ throughout the temperature range of the measurement process) which in turn is reflected as a very small capacitance value (∼pF). The behavior is akin to that observed in the case of the SSR-derived samples.

Figure 7 represents the variation of terminal capacitance as a function of frequency measured at 27 °C and 300 °C. As in the case of the SSR-derived samples, the weak temperature dependence of the terminal capacitance in the SHS-derived $SrSnO_3$ can be appreciated from this illustration. A value of ∼3.5 pF could easily be assigned to the sample capacitance over this measurement temperature range. Furthermore, the capacitance of $SrSnO_3$ possesses near-zero temperature dependence which remains very steady over 4 decades of frequency range.

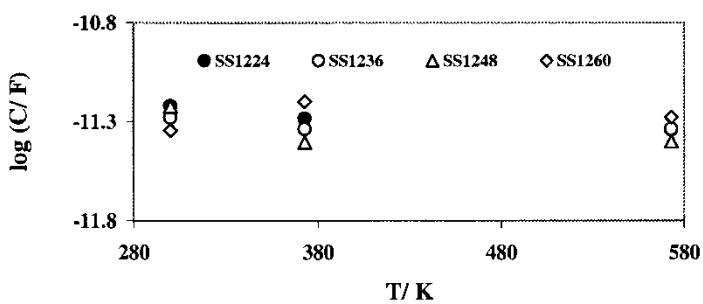
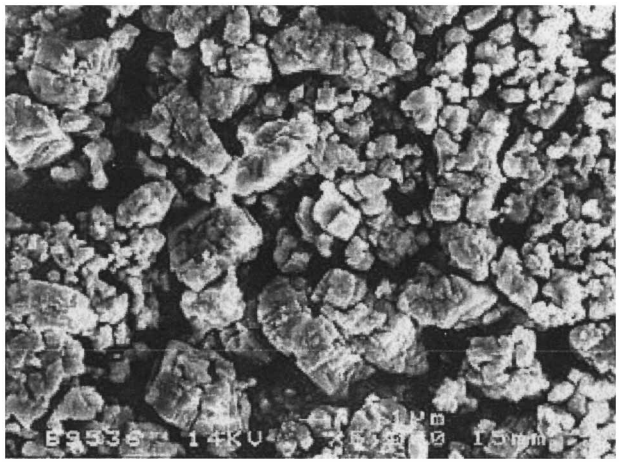


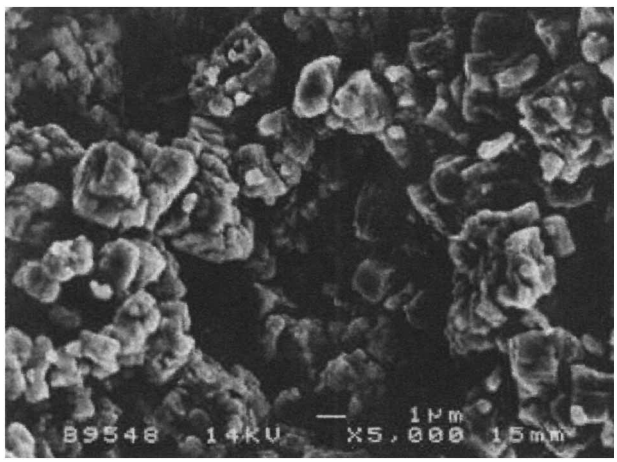
FIGURE 4 Temperature dependence of capacitance for the $SrSnO_3$ samples sintered at 1200 °C with soak-time ranging between 24 h and 60 h.

TABLE I Values of TCC and TCK Calculated over the Range 27°–300 °C from the Measured Capacitance and Geometry of the $SrSnO_3$ Ceramic Samples Sintered at Various Temperatures for Different Soak-times.

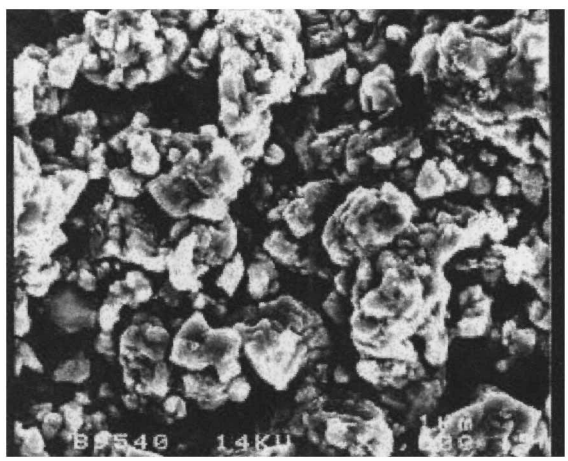
	$\ln(C/F) = a + bT/K$		$\ln k = a' + b' T/K$			
Sample History (T–t)	a	b	a'	b'	TCC (K^{-1})	TCK (K^{-1})
SSR: 1200 °C/24 h	−25.59	-9.212×10^{-4}	2.1606	-8.8622×10^{-4}	-9.2×10^{-4}	-8.86×10^{-4}
SSR: 1200 °C/36 h	−25.91	-4.606×10^{-4}	1.8836	-3.9202×10^{-4}	-4.6×10^{-4}	-3.92×10^{-4}
SSR: 1200 °C/48 h	−25.64	-1.1515×10^{-4}	2.0153	-7.6078×10^{-4}	-11.5×10^{-4}	-7.61×10^{-4}
SSR: 1200 °C/60 h	−26.07	$+2.303 \times 10^{-4}$	1.8977	-6.4955×10^{-5}	$+2.3 \times 10^{-4}$	-6.50×10^{-5}
SSR: 1350 °C/12 h	−26.62	$+2.073 \times 10^{-4}$	1.0661	$+3.4133 \times 10^{-4}$	$+2.1 \times 10^{-4}$	$+3.41 \times 10^{-4}$
SHS: 1350 °C/2 h	−25.96	-6.909×10^{-4}	1.9504	-9.7950×10^{-4}	-6.91×10^{-4}	-9.80×10^{-4}
SHS: 1350 °C/6 h	−25.50	-6.909×10^{-4}	2.1583	-4.9228×10^{-4}	-6.91×10^{-4}	-4.93×10^{-4}
SHS: 1350 °C/12 h	−25.62	-9.212×10^{-4}	2.0404	-9.0582×10^{-5}	-9.21×10^{-4}	-9.06×10^{-5}



(a)



(b)



(c)

FIGURE 5 Microstructure of the SSR-derived $SrSnO_3$ material system sintered at 1200 °C with soak-time (a) 24 h, (b) 36 h, (c) 48 h, and (d) 60 h.

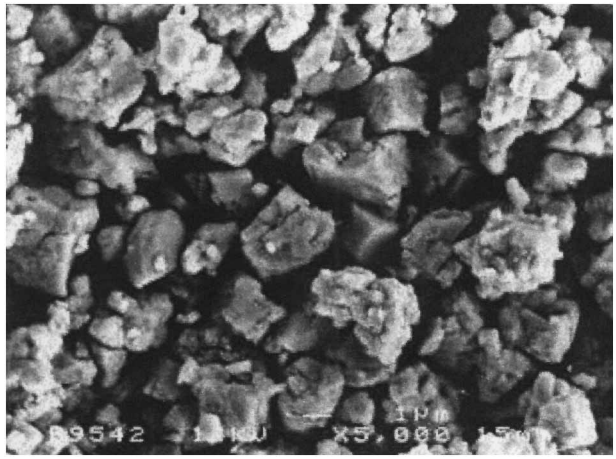


FIGURE 5 (Continued)

The temperature dependence of the relative dielectric constant selected at a measurement frequency corresponding to the steady regime is shown in the form of the straight line in Figure 8. The parametric equations representing temperature dependence of the terminal capacitance and the relative dielectric constant in conjunction with the computed values of TCC and TCK are documented in Table I. Overall, the device capacitance varies within a very narrow band in the measurement temperature range.

The parametric equations for the electrical data of the SHS-derived samples sintered at 1350 °C for various soak-times (>2 h) are also shown in Table I. The microstructure of this sample sintered at 1350 °C with soak-time 12 h is shown in Figure 9.

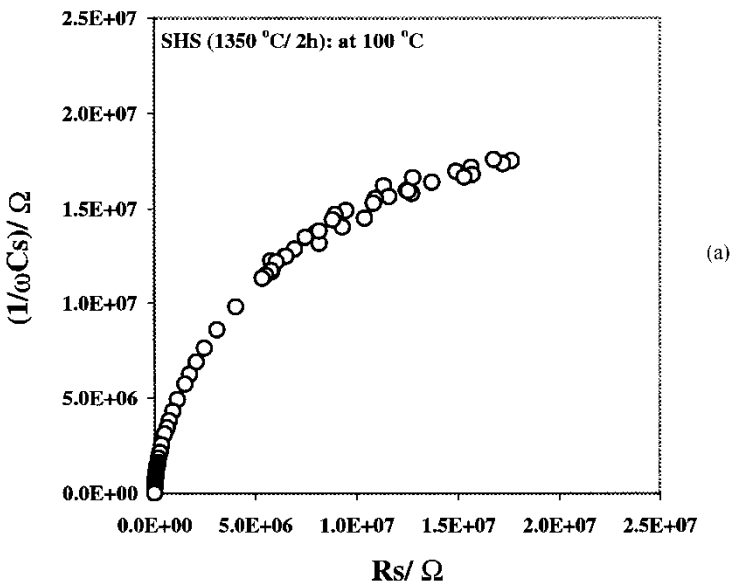


FIGURE 6 Complex plane plots for the $SrSnO_3$ samples synthesized via SHS route. (a) Impedance (Z*) plot for the sample sintered at 1350 °C with soak-time 2 h measured at 100 °C, (b) complex capacitance plot (C*) plot for the same sample as in (a) measured at 27 °C, (c) modulus (M*) plot of the same data as in (b).

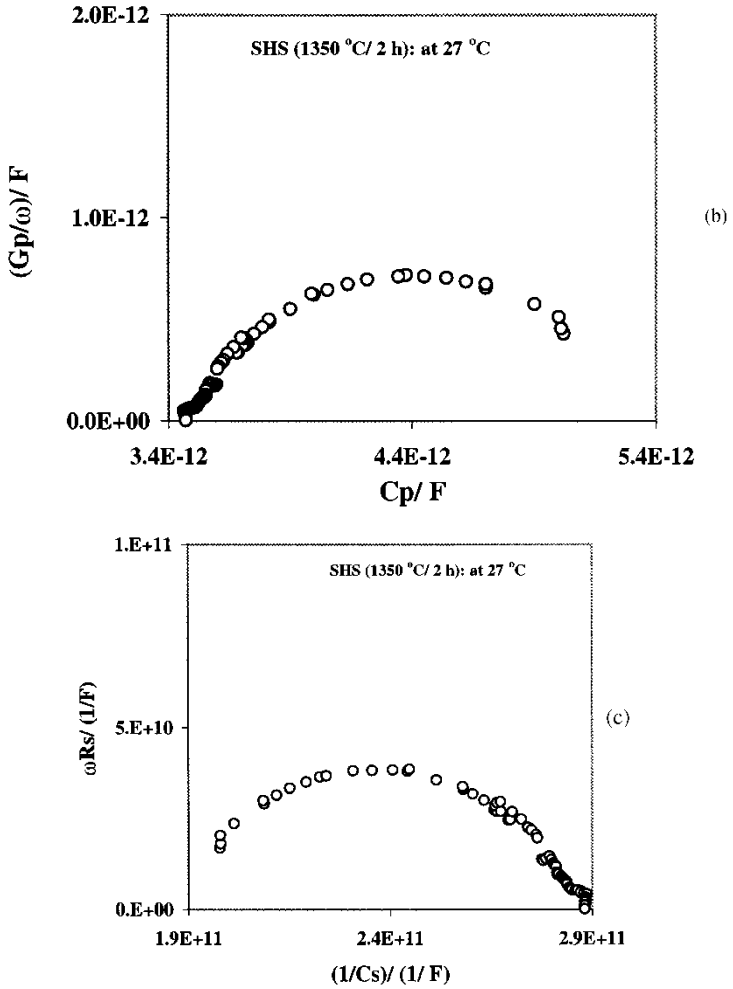


FIGURE 6 (Continued)

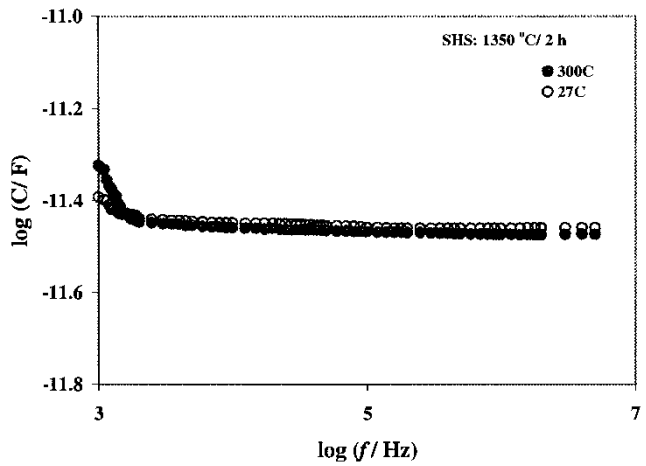


FIGURE 7 Frequency dependence of capacitance of the SHS-derived $SrSnO_3$ samples sintered at 1350 °C for 2 h.

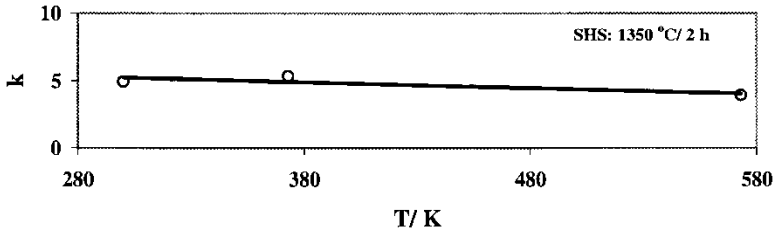


FIGURE 8 Temperature dependence of the relative dielectric constant of SHS-derived $SrSnO_3$ samples sintered at 1350 °C for 2 h.

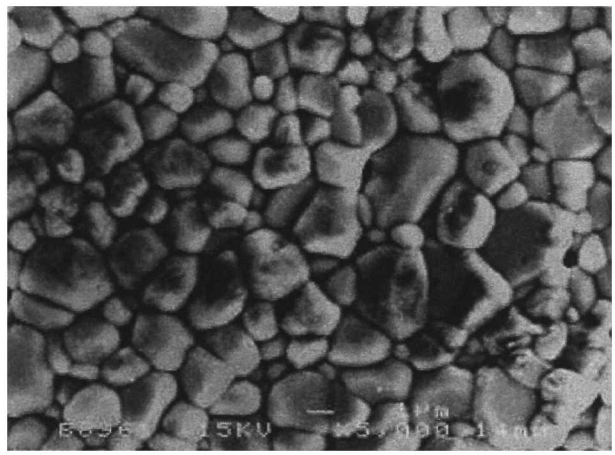


FIGURE 9 Microstructure of the SRS-derived $SrSnO_3$ sample sintered at 1350 °C with soak-time 12 h.

A comparison of the parametric equations derived for the SSR and SHS samples sintered at various T–t schedules yields an interesting feature. In the case of SSR-derived samples, the TCC is negative for the samples sintered up to 48 h soak-time while it becomes positive at higher soak-times (such as 1200 °C for 60 h). In the case of SHS-derived samples, the switchover from negative to positive TCC takes place in the samples sintered at 1350 °C for soak-time more than 12 h. This behavior could be attributed to the systematic evolution of the microstructural features with increasing soak-time at a given temperature. In the light of this systematic and progressive trend, it is more than likely to obtain a capacitor component with the $SrSnO_3$ possessing either zero or very near zero TCC. This can be achieved using an appropriate sintering schedule for the samples employing either of the two processing techniques.

4 EQUIVALENT CIRCUIT MODEL

In the light of the foregoing data-handling criteria, a systematic equivalent circuit analog can be developed. The multi-plane analytical technique provided methodical extraction of the circuit elements which can be incorporated in the model presented in Figure 10. Based on Z*- and M*-plane analyses a voltage dividing configuration consisting of the R–C parallel combination can be erected. The lumped single-like relaxation process obtained in the

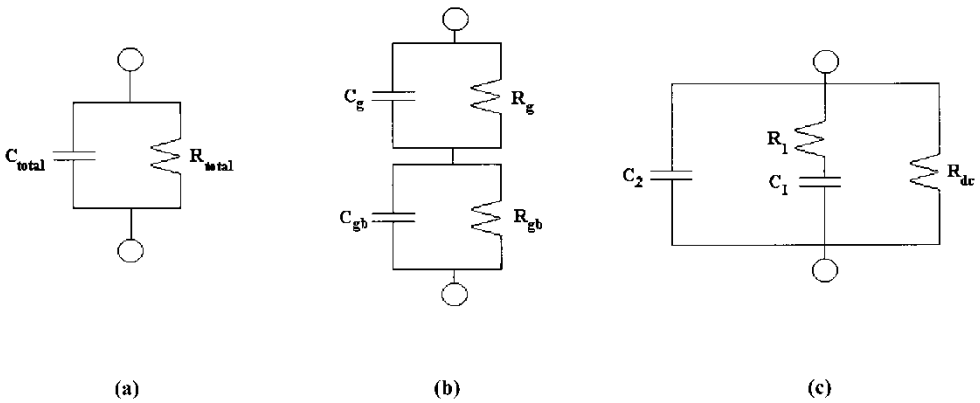


FIGURE 10 Equivalent circuit model: (a) elements extracted as absolute lumped elements obtained in the Z*-plane, (b) elements extracted as a voltage dividing configuration obtained in the M*-plane, (c) trapping response within the grain-boundary depletion regions obtained in the C*-plane.

Z*-plane yielded only R–C parallel combination denoted as R_{total}–C_{total} in Figure 10a. Such a lumped parallel combination is a simplified view of any electrically active material system. The real picture of this represention is more complicated than it appeared in the Z*-plane. It is needless to say that if the investigation is confined within a single complex plane formalism (such as Z*-plane), the investigator would terminate interpretation with a limited explanation or information for the audience. Therefore, additional analysis via other complex plane formalism(s) will certainly be conducive to the investigators exploiting this approach of the analytical method. Nevertheless, R_{total} and C_{total} indicate the dc condition (i.e., $f \rightarrow 0$ Hz) of the capacitor component shown in Figure 10a. In this case both R_{total} and C_{total} are the frequency-independent parameters. They represent absolute lumped grain-boundary depletion contribution and single-like bulk dielectric response. Here, the concept of absolute lumped means the single lumped resistance as well as single lumped capacitance which cannot be further lumped.

When two overlapped or consecutive relaxations are present for the same set of the a.c. electrical data, it implies that there should be two voltage dividing R–C parallel combinations in series. Such relaxations are evident in the M*-plane plots and, therefore, the corresponding equivalent circuit analog requires a modification when compared to that obtained in the Z*-plane. This modification is depicted in Figure 10b. The series configuration of the two R–C parallel combinations relates to an extended mechanism which was masked by the Z*-plane analysis. Thus, the M*-plane plot is probing to an additional feature for the same data. Each segment of the series configuration consists of the R–C parallel components. Thus, two segments consisting of R_g–C_g and R_{gb}–C_{gb} in series configuration can be visualized. The low-frequency response yields the relaxation consisting of the R_{gb}–C_{gb} where R_{gb} represents the lumped resistance associated with the grain-boundary and C_{gb} represents the corresponding lumped capacitance. In the same way, the high-frequency response yields the relaxation consisting of the R_g–C_g where R_g is the lumped resistance and C_g is the lumped capacitance of the grains. Thus, the lumped grains and grain-boundaries within the microstructures can be simplified [6, 7, 18, 19].

In order to achieve a completeness of the equivalent circuit model it is essential that the trapping states at the grain-boundary interfaces should be taken into consideration. This behavior is totally masked either in the Z*-plane plot or in the M*-plane plot. Usually trapping states may contribute when they lie within the electric field falling regions. Such a contribution is supported by the C*-plane relaxation where the trapping response is a series

event [10–16] represented by the R_1–C_1 combination. Also, in this case a concept of barrier layer (grain-boundary depletion contribution and single-like bulk dielectric response) capacitance (C_2) is construed in conjunction with a dc leakage resistance (R_{dc}) as this material system is not a perfect insulator. Such a configuration can be visualized with a current dividing equivalent circuit configuration depicted in Figure 10c. Such a configuration was employed effectively for the ZnO-based varistor materials [16].

The multi-fold perspective of an equivalent circuit model ultimately reduces to a singular (unified) nature of the total conduction across the sample (i.e., between the electrodes). It is a matter of analytical mind and viewing perspective of the unknown device under test (DUT) for an investigator who would decide the importance of the extracted parameter(s). An unknown DUT or a material system when examined thus ascertains the applications criteria based on the evaluation of the extracted parameters from a choice of analytical method. Therefore, each of the equivalent circuit models provided within Figure 10 is interchangeable. Any one of them is representable depending on the experimental situation. The experimental limitation, capability, visibility, etc. including the window of investigation will allow the ultimate choice of the model. Often one of these models can be presented alone only with a limited interpretation. Nevertheless, each mode of interpretation corresponding to each circuit model is somewhat complete by itself. When all the four complex plane formalisms in conjunction with the Bode plots are fully exploited, a complete picture of the DUT can be visualized. In this way, the multi-fold representation of the equivalent circuit model converges to a single circuit configuration as the underlying contributing elements are physically located, and comprehended of their purpose as an individual contributing element which emerges from a specific behavior.

5 CONCLUSIONS

The $SrSnO_3$ based material has been synthesized via SSR and SHS routes. The capacitor components were fabricated employing a broad range of sintering schedule in the temperature ranging between 1200 °C to 1350 °C with soak-time 2 h through 60 h. A thorough analysis of the a.c. electrical data utilizing multiple complex plane analytical technique for these samples revealed simultaneous relaxation. Additional temperature-dependent data analyses yielded ultra-low TCC as well as TCK for these samples in the temperature ranging between 27 °C and 300 °C. Furthermore, nearly constant values of these two parameters were achieved over a wide range of measurement frequency. This frequency range extends to nearly 4 decades. Thus, the $SrSnO_3$-based material system has a strong potential of being exploited as a low capacitance but high resistance component including very low TCC and TCK properties for a variety of electronic applications.

The concurrent multi-plane analytical approach has been found to be effective in determining applicability of a device system for electronic applications. The results were further supported by the Bode plots. Overall, the way a.c. electrical data have been handled, analyzed, and parameters extracted to understand their role within the microstructures, has provided a broader aspect of the immittance spectroscopy. Such in-depth investigation as well as the extraction of the electrical circuit elements at various situations provides an insight into the material behavior.

The invariant nature of the TCC and TCK indicate that the $SrSnO_3$-based material system is likely to exhibit less sensitivity of the trapping effect with respect to the elevation of the ambient temperature. Thus, it is believed that the TCC and TCK properties are established for a potentially new application as a circuit element.

References

[1] Herbert, J. M. (1985). Ceramic Dielectrics and Capacitors. Gordon and Breach Science Publishers, Philadelphia.
[2] Furuta, N. (1998). Asian Electron. Indust., 3, 64.
[3] Azad, A.-M. (1997). In: Khan, M. A., Haq, A., Hussain, K. and Khan, A. Q. (Eds.), Proceedings of the 5th International Symposium on Advanced Materials, 21–25 September, 1997, Islamabad, Pakistan, Dr. A. Q. Khan Research Laboratories, Kahuta, Pakistan, pp. 110–117.
[4] Azad, A.-M. and Hon, N. C. (1998). J. Alloys Comp., 270, 95.
[5] Azad, A.-M., Shyan, L. L. W. and Yen, P. T. (1999). J. Alloys Comp., 282, 101.
[6] Azad, A.-M., Shyan, L. L. W. and Alim, M. A. (1999). J. Mater. Sci., 34, 1175.
[7] Azad, A.-M., Shyan, L. L. W. and Alim, M. A. (1999). J. Mater. Sci., 34, 3375.
[8] Parkash, O., Mandal, K. D., Christopher, C. C., Sastry, M. S. and Kumar, D. (1994). J. Mater. Sci. Lett., 13, 1616.
[9] Alim, M. A. and Akbar, S. A. (1992). Immittance Data Acquisition and Analytical Software Package, Developed at The Ohio State University, Columbus, Ohio.
[10] Alim, M. A. (1996). Act. Pass. Electron. Comp., 19, 139.
[11] Alim, M. A. (1996). Materials Research Society Proceedings: Electrically-Based Microstructural Characterization, 411, 13.
[12] Alim, M. A. (1996). Materials Research Society Proceedings: Electrically-Based Microstructural Characterization, 411, 113.
[13] Alim, M. A. (1989). J. Am. Ceram. Soc., 72, 28.
[14] Alim, M. A. (1994). Act. Pass. Electron. Comp., 17, 99–118.
[15] Alim, M. A. (1994). Act. Pass. Electron. Comp., 17, 57–65.
[16] Alim, M. A., Seitz, M. A. and Hirthe, R. W. (1988). J. Appl. Phys., 63, 2337.
[17] Alim, M. A. (1993). J. Appl. Phys., 74, 5850.
[18] Hodge, I. M., Ingram, M. D. and West, A. R. (1975). J. Electroanal. Chem., 58, 429.
[19] Sinclair, D. C. and West, A. R. (1989). J. Appl. Phys., 66, 3850.